

TRS213 5V Multichannel RS-232 Line Driver and Receiver with $\pm 15\text{kV}$ ESD Protection

1 Features

- ESD Protection for RS-232 bus pins
 - $\pm 15\text{kV}$ Human-body model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates at 5V V_{CC} supply
- Four drivers and five receivers
- Operates up to 120kbit/s
- Low supply current in shutdown mode: 15 μA typical
- External Capacitors: 4 $\times$ 0.1 μF
- Designed to be interchangeable with industry standard '213 devices
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- [Battery-powered systems](#)
- [PDAs](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

3 Description

The TRS213 device consists of four line drivers, five line receivers, and a dual charge-pump circuit with $\pm 15\text{kV}$ ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5V supply. The devices operate at data signaling rates up to 120kbit/s and a maximum of 30V/ μs driver output slew rate.

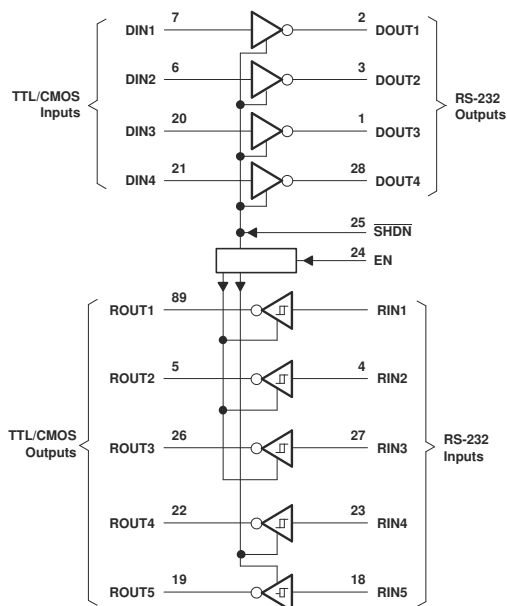
The TRS213 has an active-low shutdown ($\overline{\text{SHDN}}$) and an active-high enable control (EN). In shutdown mode, the charge pumps are turned off, V^+ is pulled down to V_{CC} , V^- is pulled to GND, and the transmitter outputs are disabled. This reduces supply current typically to 1 μA . Two receivers of the TRS213 are active during shutdown.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TRS213	DB (SSOP)	10.2 mm x 7.8mm
	DW (SOIC)	17.9mm x 10.3mm

(1) For more information, see [Section 11](#).

(2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

**DB, DW, OR PW PACKAGE
(TOP VIEW)**

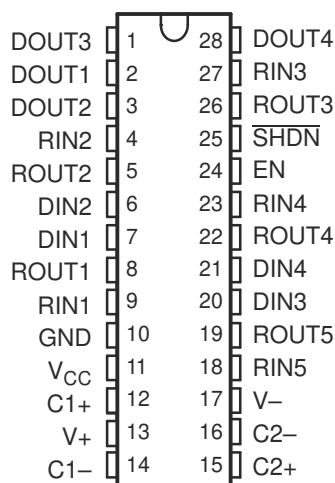


Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
DOUT3	1	O	RS-232 driver outputs
DOUT1	2	O	RS-232 driver outputs
DOUT2	3	O	RS-232 driver outputs
RIN2	4	I	RS-232 receiver input
ROUT2	5	O	Receiver output
DIN2	6	I	Driver inputs
DIN1	7	I	Driver inputs
ROUT1	8	O	Receiver output
RIN1	9	I	RS-232 receiver input
GND	10	-	Ground
V _{CC}	11	-	Supply voltage
C1+	12	-	Positive terminal of the voltage-doubler charge-pump capacitor
V+	13	-	Positive charge pump output voltage
C1-	14	-	Negative terminal of the voltage-doubler charge-pump capacitor
C2+	15	-	Positive terminal of the voltage-doubler charge-pump capacitor
C2-	16	-	Negative terminal of the voltage-doubler charge-pump capacitor
V-	17	-	Negative charge pump output voltage
RIN5	18	I	RS-232 receiver input
ROUT5	19	O	Receiver output
DIN3	20	I	Driver inputs
DIN4	21	I	Driver inputs
ROUT4	22	O	Receiver output
RIN4	23	I	RS-232 receiver input

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
EN	24	I	Active high enable
SHDN	25	I	Active low shutdown
ROUT3	26	O	Receiver output
RIN3	27	I	RS-232 receiver input
DOUT4	28	O	RS-232 driver outputs

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.3	6	V
V+	Positive charge-pump voltage range ⁽²⁾	V _{CC} − 0.3	14	V
V−	Negative charge-pump voltage range ⁽²⁾	0.3	−14	V
V _I	Input voltage range	Drivers	−0.3 V+ + 0.3	V
		Receivers (DB Package)	±25	
		Receivers (DW Package)	±30	V
V _O	Output voltage range	Drivers	V− − 0.3 V+ + 0.3	V
		Receivers	−0.3 V _{CC} + 0.3	
DOUT	Short-circuit duration	Continuous		
T _J	Operating virtual junction temperature	150		C°
T _{stg}	Storage temperature range	−65	150	C°

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 Recommended Operating Conditions

See Figure 6-4, and note ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage			4.5	5	5.5	V
V _{IH}	Driver high-level input voltage	DIN	2			V
	Control high-level input voltage	EN, $\overline{\text{SHDN}}$	2.4			
V _{IL}	Driver and control low-level input voltage	DIN, EN, $\overline{\text{SHDN}}$			0.8	V
V _I	Driver and control input voltage	DIN, EN, $\overline{\text{SHDN}}$	0		5.5	V
		RIN (DB package)	–25		25	
	Receiver input voltage	RIN (DW package)	–30		30	V
T _A	Operating free-air temperature	TRS213C	0		70	°C
		TRS213I	–40		85	

- (1) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		DW (SOIC)	DB (SSOP)	UNIT
		28 PINS	28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	72.3	66.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	33.5	33.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	37.1	37.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.5	4.6	°C/W

5.3 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾	DW (SOIC)	DB (SSOP)	UNIT
	28 PINS	28 PINS	
Ψ_{JB} Junction-to-board characterization parameter	37.1	36.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC} Supply current	No load, See Figure 8-1		14	20	mA
I _{SHDN} Shutdown supply current	T _A = 25°C, See Figure 6-1		15	50	μA

(1) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.5 Electrical Characteristics, Driver

over operating free-air temperature range (unless otherwise noted) (see Figure 6-4, and note ⁽³⁾)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH} High-level output voltage	DOUT at R _L = 3 kΩ to GND	5	9		V
V _{OL} Low-level output voltage	DOUT at R _L = 3 kΩ to GND	–5	–9		V
I _{IH} Control high-level input current	EN, $\overline{\text{SHDN}}$ = 5V		3	10	μA
I _{IL}	Driver low-level input current		–15	–200	μA
	Control low-level input current		–3	–10	
I _{OS} ⁽²⁾ Short-circuit output current	V _{CC} = 5.5V, V _O = 0V		±10	±60	mA
r _o Output resistance	V _{CC} , V ₊ , and V _– = 0V, V _O = ±2V	300			Ω

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5V

5.6 Switching Characteristics, Driver

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate	C _L = 50pF to 1000pF, R _L = 3kΩ to 7kΩ, One DOUT switching, See Figure 6-3	120			kbit/s
t _{PLH(D)} Propagation delay time, low- to high-level output	C _L = 2500pF, R _L = 3kΩ, All drivers loaded, See Figure 6-3		2		μs
t _{PHL(D)} Propagation delay time, high- to low-level output	C _L = 2500pF, R _L = 3kΩ, All drivers loaded, See Figure 6-3		2		μs
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 150pF to 2500pF, R _L = 3kΩ to 7kΩ, See Figure 6-3		300		ns
SR(tr) Slew rate, transition region (see Figure 6-2)	C _L = 50pF to 1000pF, V _{CC} = 5V, R _L = 3kΩ to 7kΩ	3	6	30	V/μs

(1) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.

(3) Pulse skew is defined as (t_{PLH} – t_{PHL}) of each channel of the same device.

5.7 ESD Protection, Driver

over operating free-air temperature range (unless otherwise noted)

PIN	TEST CONDITIONS	TYP	UNIT
DOUT	Human-Body Model	±15	kV

5.8 Electrical Characteristics, Receiver

over operating free-air temperature range (unless otherwise noted) (see Figure 8-1), and see note⁽³⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = –1mA	V _{CC} – 0.4			V
V _{OL} Low-level output voltage	I _{OH} = 1.6mA	0.4			V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 5V, T _A = 25°C	Active mode		1.7	2.4
		Shutdown mode (R4–R5)		1.5	2.4
V _{IT–} Negative-going input threshold voltage	V _{CC} = 5V, T _A = 25°C	Active mode		0.8	1.2
		Shutdown mode (R4–R5)		0.6	1.5
V _{hys} ⁽²⁾ Input hysteresis (V _{IT+} , V _{IT–})	V _{CC} = 5V	0.5			1
r _I Input resistance	V _{CC} = 5V, T _A = 25°C	3	5	7	kΩ
Output leakage current	EN = 0V, 0 ≤ ROUT ≤ V _{CC} , R1–R3	±0.05			±10
					μA

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.

(2) No hysteresis in shutdown mode

(3) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5 V.

5.9 Switching Characteristics, Receiver

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
t _{PLH(R)} Propagation delay time, low- to high-level output	C _L = 150pF, See Figure 6-4	SHDN = V _{CC}		0.5	10
		SHDN = 0V, R4–R5		4	40
t _{PHL(R)} Propagation delay time, high- to low-level output	C _L = 150pF, See Figure 6-4			0.5	10
t _{en} Output enable time	C _L = 150pF, See Figure 6-5			600	ns
t _{dis} Output disable time	C _L = 150pF, See Figure 6-5			200	ns

(1) Test conditions are C1–C4 = 0.1μF at V_{CC} = 5V ± 0.5V.

(2) All typical values are at V_{CC} = 5V, and T_A = 25°C.

5.10 ESD Protection, Receiver

over operating free-air temperature range (unless otherwise noted)

PIN	TEST CONDITIONS	TYP	UNIT
RIN	Human-Body Model	±15	kV

6 Parameter Measurement Information

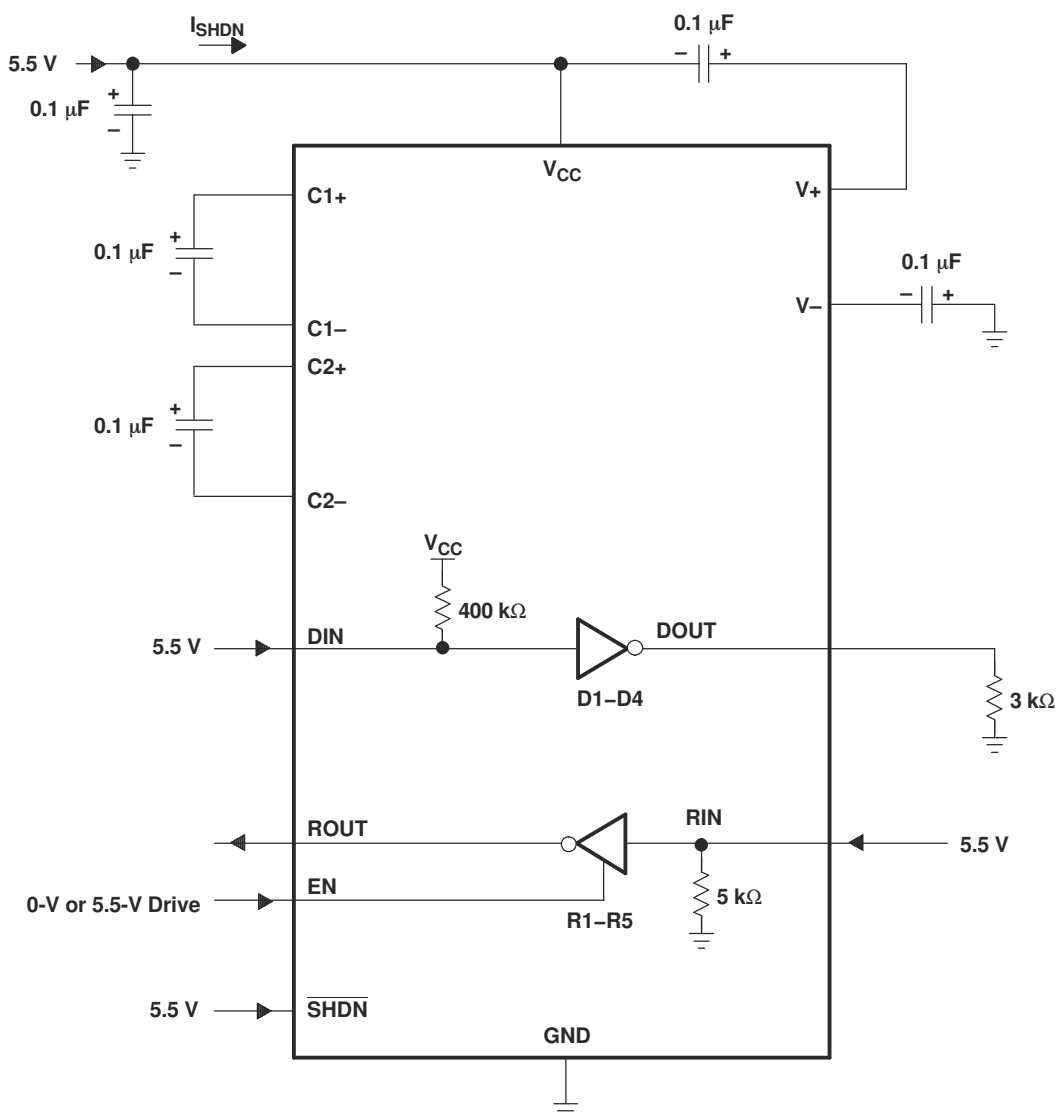
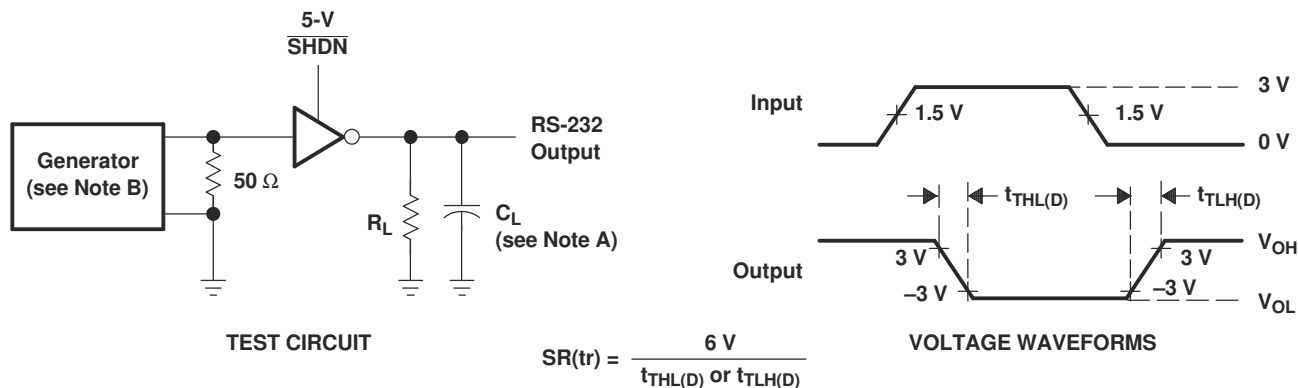


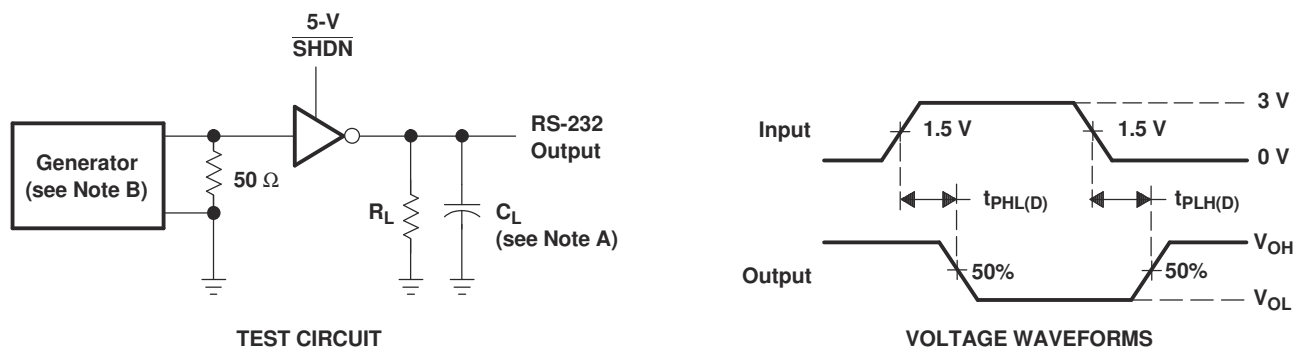
Figure 6-1. Shutdown Current Test Circuit



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

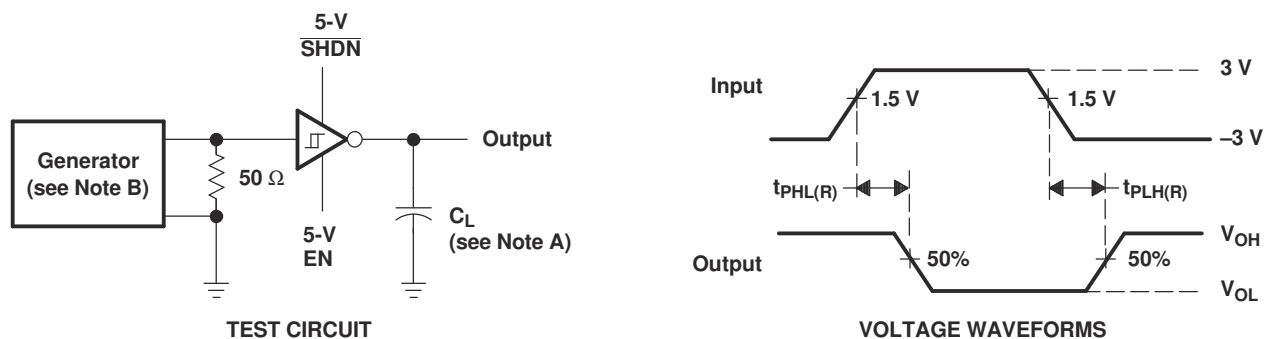
Figure 6-2. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

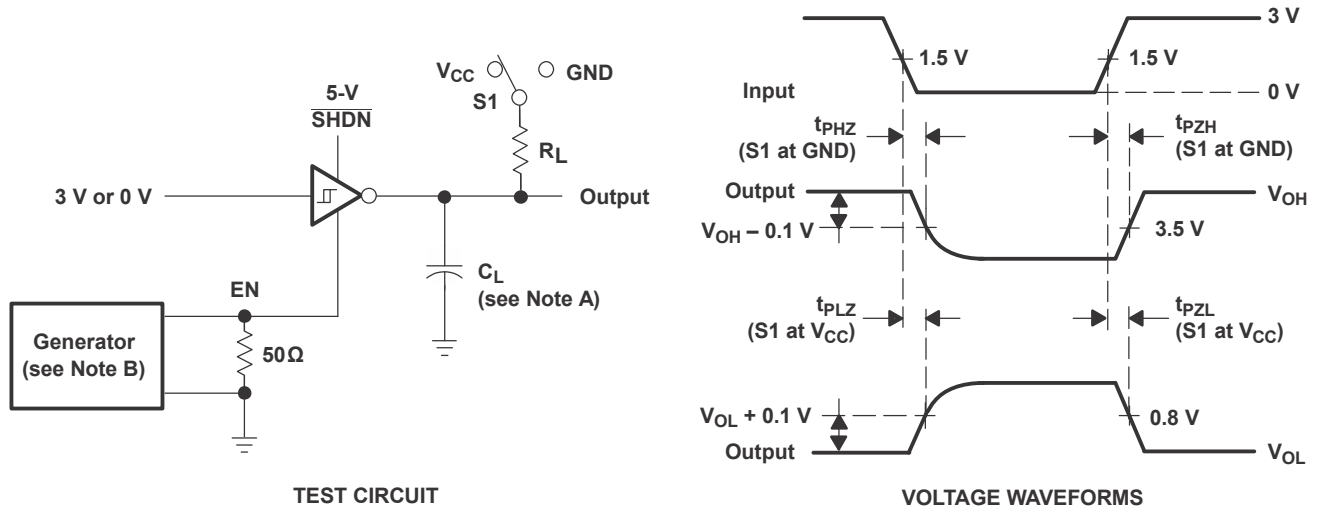
Figure 6-3. Driver Pulse Skew and Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 6-4. Receiver Propagation Delay Times



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\ \text{ns}$, $t_f \leq 10\ \text{ns}$.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 6-5. Receiver Enable and Disable Times

7 Functional Modes

Table 7-1. Function Table

INPUTS		DRIVER D1–D4	RECEIVER		DEVICE STATUS
SHDN	EN		R1–R3	R4–R5	
L	L	Z	Z	Z	Shutdown
L	H	Z	Z	Active ⁽¹⁾	Shutdown
H	L	All active	Z	Z	Normal operation
H	H	All active	Active	Active	Normal operation

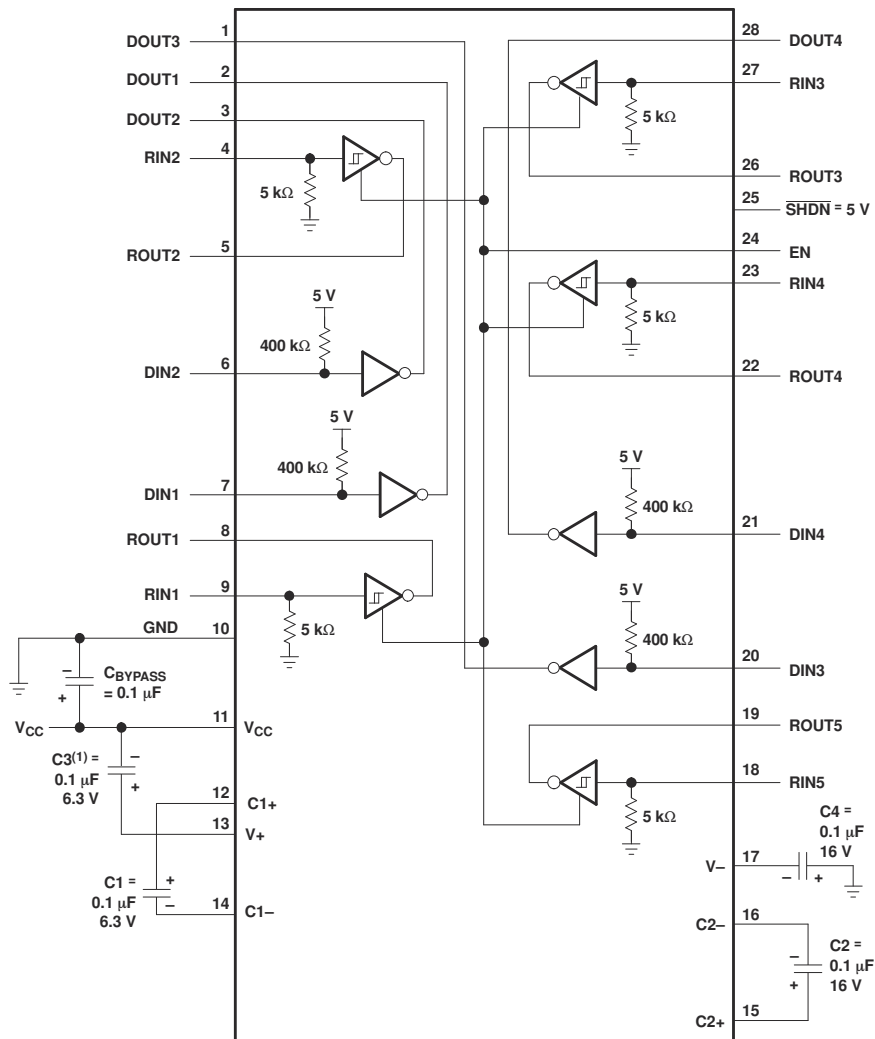
(1) See the V_{IT+} and V_{IT-} change in the *Electrical Characteristics* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8-1. Typical Operating Circuit and Capacitor Values

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2007) to Revision A (July 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed the DB package Input voltage range for Receivers from $\pm 30V$ to $\pm 25V$ in the <i>Absolute Maximum Ratings</i> and the <i>Recommended Operating Conditions</i>	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS213CDBR	Obsolete	Production	SSOP (DB) 28	-	-	Call TI	Call TI	0 to 70	TRS213C
TRS213IDB	Obsolete	Production	SSOP (DB) 28	-	-	Call TI	Call TI	-40 to 85	TRS213I
TRS213IDBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I
TRS213IDBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I
TRS213IDBRG4	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I
TRS213IDBRG4.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I
TRS213IDWR	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I
TRS213IDWR.A	Active	Production	SOIC (DW) 28	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS213I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS213IDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS213IDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS213IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

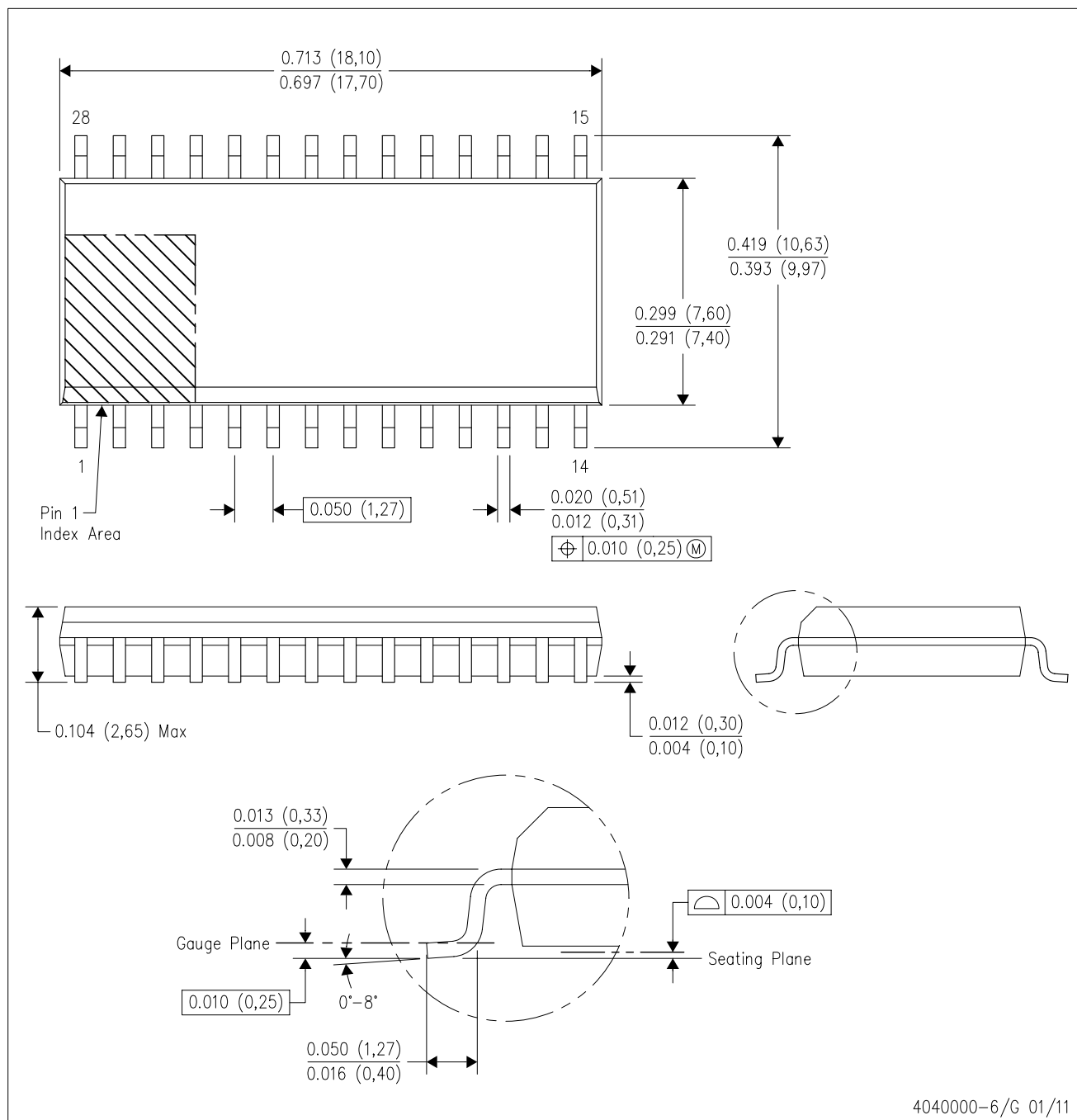


*All dimensions are nominal

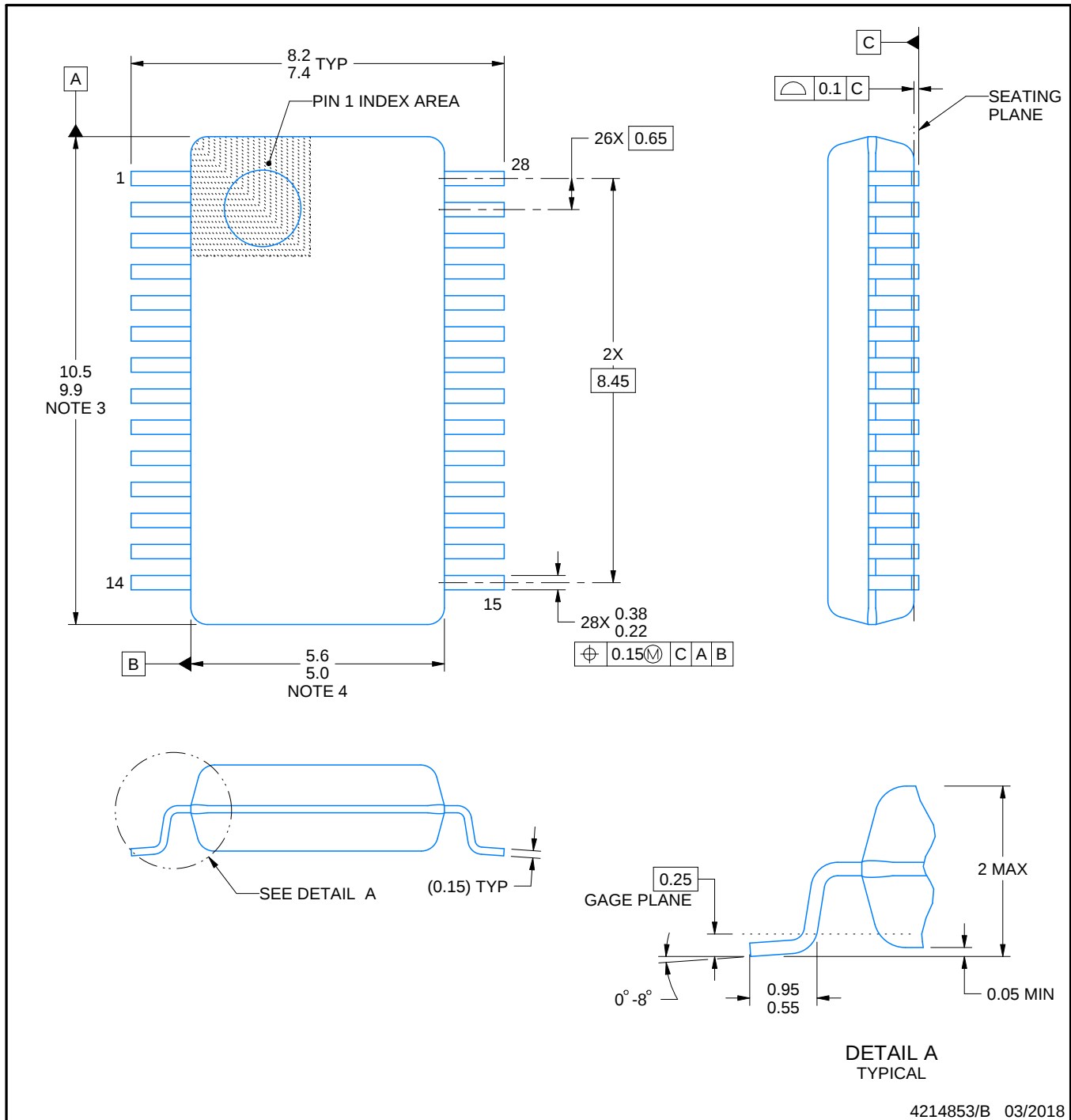
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS213IDBR	SSOP	DB	28	2000	353.0	353.0	32.0
TRS213IDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0
TRS213IDWR	SOIC	DW	28	1000	350.0	350.0	66.0

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.



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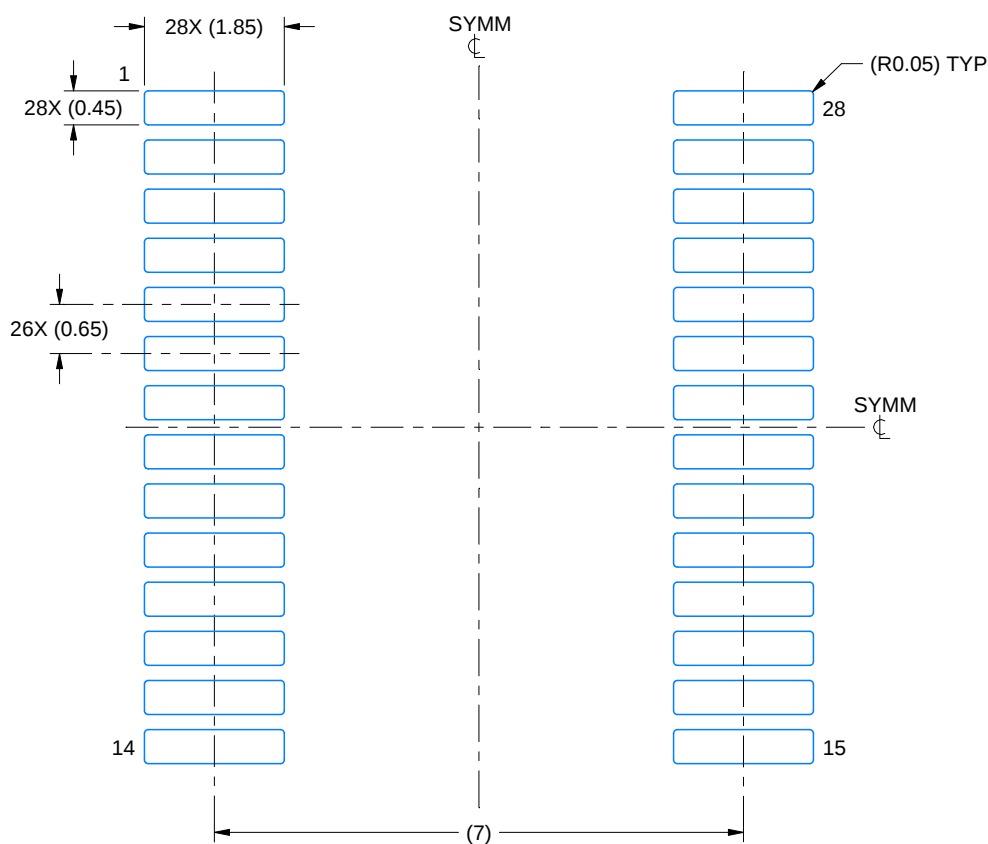
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

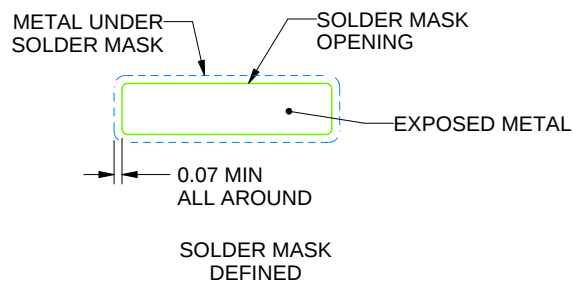
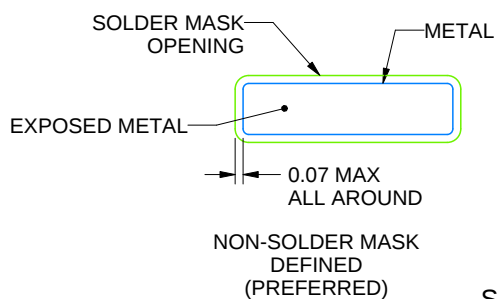
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

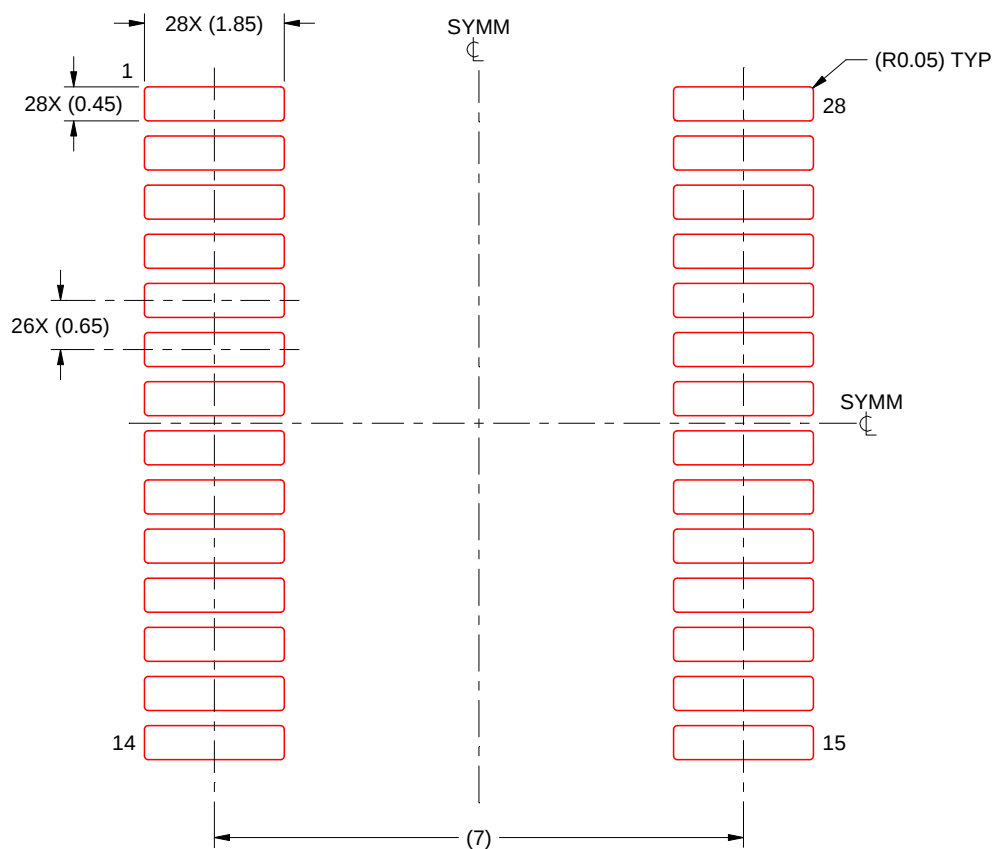
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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