

DS92LV010A Bus LVDS 3.3/5.0V Single Transceiver

Check for Samples: [DS92LV010A](#)

FEATURES

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Balanced Output Impedance
- Lite Bus Loading 5pF Typical
- Glitch Free Power Up/Down (Driver Disabled)
- 3.3V or 5.0V Operation
- $\pm 1\text{V}$ Common Mode Range
- $\pm 100\text{mV}$ Receiver Sensitivity
- High Signaling Rate Capability (Above 100 Mbps)
- Low Power CMOS Design
- Product Offered in 8 Lead SOIC Package
- Industrial Temperature Range Operation

DESCRIPTION

The DS92LV010A is one in a series of transceivers designed specifically for the high speed, low power proprietary bus backplane interfaces. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. To minimize bus loading the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility as 4 separate lines are provided (DIN, DE, $\overline{\text{RE}}$, and ROUT). The device also features flow through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10 mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27 Ohms.

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of $\pm 1\text{V}$.

The receiver threshold is $\pm 100\text{mV}$ over a $\pm 1\text{V}$ common mode range and translates the low voltage differential levels to standard (CMOS/TTL) levels.

CONNECTION DIAGRAM

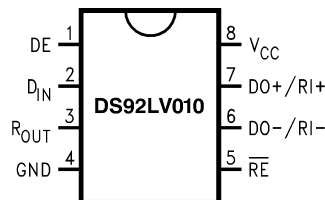


Figure 1. SOIC Package
See Package Number D0008A

BLOCK DIAGRAM

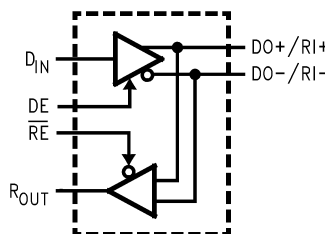


Figure 2.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾⁽³⁾

Supply Voltage (V_{CC})		6.0V
Enable Input Voltage (DE, $\overline{RE}$)		-0.3V to ($V_{CC} + 0.3V$)
Driver Input Voltage (DIN)		-0.3V to ($V_{CC} + 0.3V$)
Receiver Output Voltage (R_{OUT})		-0.3V to ($V_{CC} + 0.3V$)
Bus Pin Voltage (DO/RI±)		-0.3V to + 3.9V
Driver Short Circuit Current		Continuous
ESD (HBM 1.5 k Ω , 100 pF)		>2.0 kV
Maximum Package Power Dissipation at 25°C	SOIC	1025 mW
	Derate SOIC Package	8.2 mW/°C
Junction Temperature		+150°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)		260°C

- (1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD} , V_{ID} , V_{TH} and V_{TL} unless otherwise specified.
- (2) Absolute Maximum Ratings are those beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of “[Electrical Characteristics](#)” provides conditions for actual device operation.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Max	Units
Supply Voltage (V_{CC}), or	3.0	3.6	V
Supply Voltage (V_{CC})	4.5	5.5	V
Receiver Input Voltage	0.0	2.9	V
Operating Free Air Temperature	-40	+85	°C

3.3V DC ELECTRICAL CHARACTERISTICS ⁽¹⁾⁽²⁾

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise noted, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V _{OD}	Output Differential Voltage	R _L = 27Ω, See Figure 3		DO+/RI+, DO-/RI-	140	250	360	mV
ΔV _{OD}	V _{OD} Magnitude Change					3	30	mV
V _{OS}	Offset Voltage				1	1.25	1.65	V
ΔV _{OS}	Offset Magnitude Change					5	50	mV
I _{OSD}	Output Short Circuit Current	V _O = 0V, DE = V _{CC}				-12	-20	mA
V _{OH}	Voltage Output High	V _{ID} = +100 mV	I _{OH} = -400 μA	R _{OUT}	2.8	3		V
		Inputs Open			2.8	3		V
		Inputs Shorted			2.8	3		V
		Inputs Terminated, R _L = 27Ω			2.8	3		V
V _{OL}	Voltage Output Low	I _{OL} = 2.0 mA, V _{ID} = -100 mV				0.1	0.4	V
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V, V _{ID} = +100 mV				-5	-35	-85
V _{TH}	Input Threshold High	DE = 0V		DO+/RI+, DO-/RI-			+100	mV
V _{TL}	Input Threshold Low				-100			mV
I _{IN}	Input Current	DE = 0V, V _{IN} = +2.4V, or 0V			-20	±1	+20	μA
		V _{CC} = 0V, V _{IN} = +2.4V, or 0V			-20	±1	+20	μA
V _{IH}	Minimum Input High Voltage			DIN, DE,RE	2.0		V _{CC}	V
V _{IL}	Maximum Input Low Voltage				GND		0.8	V
I _{IH}	Input High Current	V _{IN} = V _{CC} or 2.4V				±1	±10	μA
I _{IL}	Input Low Current	V _{IN} = GND or 0.4V				±1	±10	μA
V _{CL}	Input Diode Clamp Voltage	I _{CLAMP} = -18 mA			-1.5	-0.8		V
I _{CCD}	Power Supply Current	DE = $\overline{RE}$ = V _{CC} , R _L = 27Ω		V _{CC}		13	20	mA
I _{CCR}		DE = $\overline{RE}$ = 0V				5	8	mA
I _{CCZ}		DE = 0V, $\overline{RE}$ = V _{CC}				3	7.5	mA
I _{CC}		DE = V _{CC} , $\overline{RE}$ = 0V, R _L = 27Ω				16	22	mA
C _{output}	Capacitance @ BUS Pins			DO+/RI+, DO-/RI-		5		pF

- (1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD} , V_{ID} , V_{TH} and V_{TL} unless otherwise specified.
- (2) All typicals are given for $V_{CC} = +3.3\text{V}$ or 5.0V and $T_A = +25^{\circ}\text{C}$, unless otherwise stated.

5V DC ELECTRICAL CHARACTERISTICS ⁽¹⁾⁽²⁾
 $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise noted, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

Parameter		Test Conditions		Pin	Min	Typ	Max	Units	
V _{OD}	Output Differential Voltage	R _L = 27Ω, See Figure 3		DO+/-RI+, DO-/RI-	145	270	390	mV	
ΔV _{OD}	V _{OD} Magnitude Change					3	30	mV	
V _{OS}	Offset Voltage				1	1.35	1.65	V	
ΔV _{OS}	Offset Magnitude Change					5	50	mV	
I _{OSD}	Output Short Circuit Current	V _O = 0V, DE = V _{CC}				-12	-20	mA	
V _{OH}	Voltage Output High	V _{ID} = +100 mV	I _{OH} = -400 μA	R _{OUT}	4.3	5.0		V	
		Inputs Open			4.3	5.0		V	
		Inputs Shorted			4.3	5.0		V	
		Inputs Terminated, R _L = 27Ω			4.3	5.0		V	
V _{OL}	Voltage Output Low	I _{OL} = 2.0 mA, V _{ID} = -100 mV					0.1	0.4	V
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V, V _{ID} = +100 mV				-35	-90	-130	mA
V _{TH}	Input Threshold High	DE = 0V		DO+/-RI+, DO-/RI-			+100	mV	
V _{TL}	Input Threshold Low				-100			mV	
I _{IN}	Input Current	DE = 0V, V _{IN} = +2.4V, or 0V			-20	±1	+20	μA	
		V _{CC} = 0V, V _{IN} = +2.4V, or 0V			-20	±1	+20	μA	
V _{IH}	Minimum Input High Voltage			DIN, DE, RE	2.0		V _{CC}	V	
V _{IL}	Maximum Input Low Voltage				GND		0.8	V	
I _{IH}	Input High Current	V _{IN} = V _{CC} or 2.4V				±1	±10	μA	
I _{IL}	Input Low Current	V _{IN} = GND or 0.4V				±1	±10	μA	
V _{CL}	Input Diode Clamp Voltage	I _{CLAMP} = -18 mA			-1.5	-0.8		V	
I _{CCD}	Power Supply Current	DE = $\overline{\text{RE}}$ = V _{CC} , R _L = 27Ω		V _{CC}		17	25	mA	
I _{CCR}		DE = $\overline{\text{RE}}$ = 0V				6	10	mA	
I _{CCZ}		DE = 0V, $\overline{\text{RE}}$ = V _{CC}				3	8	mA	
I _{CC}		DE = V _{CC} , $\overline{\text{RE}}$ = 0V, R _L = 27Ω				20	25	mA	
C _{output}	Capacitance @ BUS Pins			DO+/-RI+, DO-/RI-		5		pF	

- (1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD} , V_{ID} , V_{TH} and V_{TL} unless otherwise specified.
- (2) All typicals are given for $V_{CC} = +3.3\text{V}$ or 5.0V and $T_A = +25^{\circ}\text{C}$, unless otherwise stated.

3.3V AC ELECTRICAL CHARACTERISTICS ⁽¹⁾

 $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

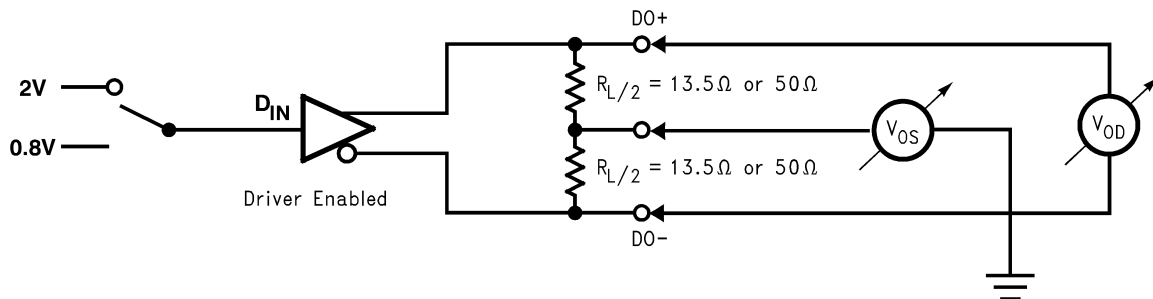
Parameter		Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t _{PHLD}	Differential Prop. Delay High to Low	R _L = 27Ω, See Figure 4 and Figure 5 C _L = 10 pF	1.0	3.0	5.0	ns
t _{PLHD}	Differential Prop. Delay Low to High		1.0	2.8	5.0	ns
t _{SKD}	Differential SKEW t _{PHLD} - t _{PLHD}			0.2	1.0	ns
t _{TLH}	Transition Time Low to High			0.3	2.0	ns
t _{THL}	Transition Time High to Low			0.3	2.0	ns
t _{PHZ}	Disable Time High to Z	R _L = 27Ω, See Figure 6 and Figure 7 C _L = 10 pF	0.5	4.5	9.0	ns
t _{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t _{PZH}	Enable Time Z to High		2.0	5.0	7.0	ns
t _{PZL}	Enable Time Z to Low		1.0	4.5	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t _{PHLD}	Differential Prop. Delay High to Low	See Figure 8 and Figure 9 C _L = 10 pF	2.5	5.0	12.0	ns
t _{PLHD}	Differential Prop. Delay Low to High		2.5	5.5	10.0	ns
t _{SKD}	Differential SKEW t _{PHLD} - t _{PLHD}			0.5	2.0	ns
t _r	Rise Time			1.5	4.0	ns
t _f	Fall Time			1.5	4.0	ns
t _{PHZ}	Disable Time High to Z	R _L = 500Ω, See Figure 10 and Figure 11 C _L = 10 pF ⁽²⁾	2.0	4.0	6.0	ns
t _{PLZ}	Disable Time Low to Z		2.0	5.0	7.0	ns
t _{PZH}	Enable Time Z to High		2.0	7.0	13.0	ns
t _{PZL}	Enable Time Z to Low		2.0	6.0	10.0	ns

- (1) Generator waveforms for all tests unless otherwise specified: $f = 1\text{MHz}$, $Z_O = 50\Omega$, $t_r, t_f \leq 6.0\text{ns}$ (0%–100%) on control pins and $\leq 1.0\text{ns}$ for RI inputs.
- (2) For receiver tri-state delays, the switch is set to V_{CC} for t_{PZL} , and t_{PLZ} and to GND for t_{PZH} , and t_{PHZ} .

5V AC ELECTRICAL CHARACTERISTICS ⁽¹⁾ $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

Parameter		Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t _{PHLD}	Differential Prop. Delay High to Low	R _L = 27Ω, See Figure 4 and Figure 5 C _L = 10 pF	0.5	2.7	4.5	ns
t _{PLHD}	Differential Prop. Delay Low to High		0.5	2.5	4.5	ns
t _{SKD}	Differential SKEW t _{PHLD} - t _{PLHD}			0.2	1.0	ns
t _{TLH}	Transition Time Low to High			0.3	2.0	ns
t _{THL}	Transition Time High to Low			0.3	2.0	ns
t _{PHZ}	Disable Time High to Z	R _L = 27Ω, See Figure 6 and Figure 7 C _L = 10 pF	0.5	3.0	7.0	ns
t _{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t _{PZH}	Enable Time Z to High		2.0	4.0	7.0	ns
t _{PZL}	Enable Time Z to Low		1.0	4.0	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t _{PHLD}	Differential Prop. Delay High to Low	See Figure 8 and Figure 9 C _L = 10 pF	2.5	5.0	12.0	ns
t _{PLHD}	Differential Prop. Delay Low to High		2.5	4.6	10.0	ns
t _{SKD}	Differential SKEW t _{PHLD} - t _{PLHD}			0.4	2.0	ns
t _r	Rise Time			1.2	2.5	ns
t _f	Fall Time			1.2	2.5	ns
t _{PHZ}	Disable Time High to Z	R _L = 500Ω, See Figure 10 and Figure 11 C _L = 10 pF ⁽²⁾	2.0	4.0	6.0	ns
t _{PLZ}	Disable Time Low to Z		2.0	4.0	6.0	ns
t _{PZH}	Enable Time Z to High		2.0	5.0	9.0	ns
t _{PZL}	Enable Time Z to Low		2.0	5.0	7.0	ns

- (1) Generator waveforms for all tests unless otherwise specified: $f = 1\text{MHz}$, $Z_O = 50\Omega$, $t_r, t_f \leq 6.0\text{ns}$ (0%–100%) on control pins and $\leq 1.0\text{ns}$ for RI inputs.
- (2) For receiver tri-state delays, the switch is set to V_{CC} for t_{PZL} , and t_{PLZ} and to GND for t_{PZH} , and t_{PHZ} .

TEST CIRCUITS AND TIMING WAVEFORMS**Figure 3. Differential Driver DC Test Circuit**

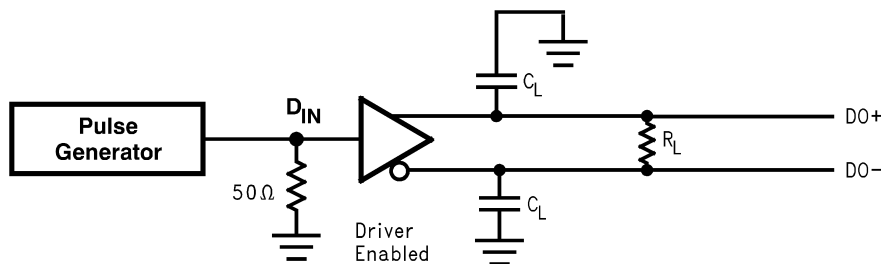


Figure 4. Differential Driver Propagation Delay and Transition Time Test Circuit

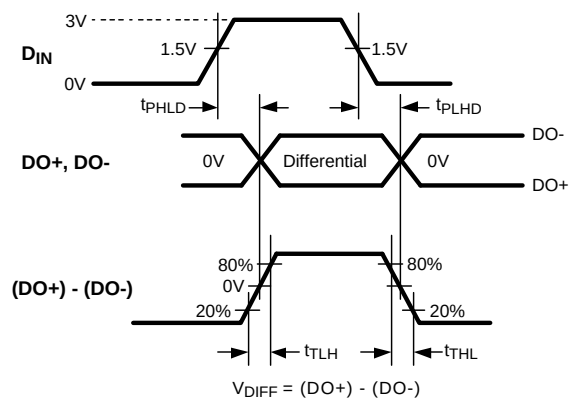


Figure 5. Differential Driver Propagation Delay and Transition Time Waveforms

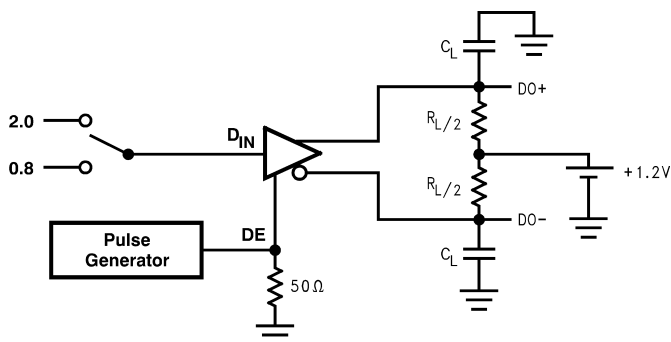


Figure 6. Driver TRI-STATE Delay Test Circuit

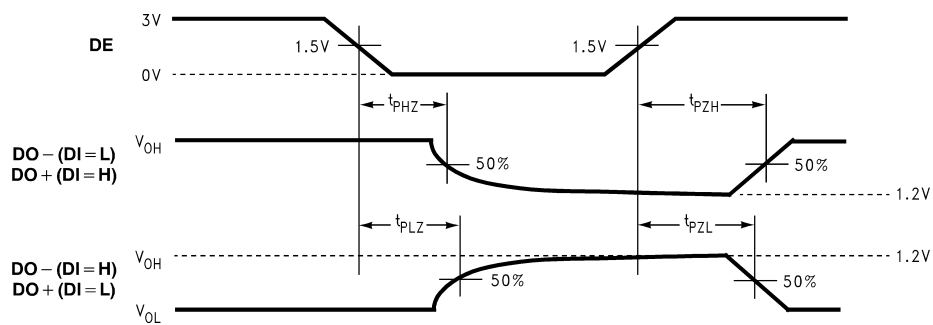


Figure 7. Driver TRI-STATE Delay Waveforms

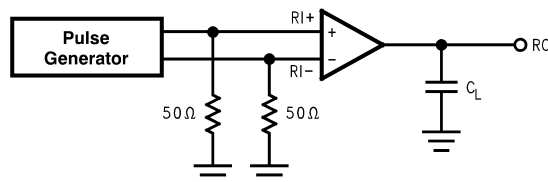


Figure 8. Receiver Propagation Delay and Transition Time Test Circuit

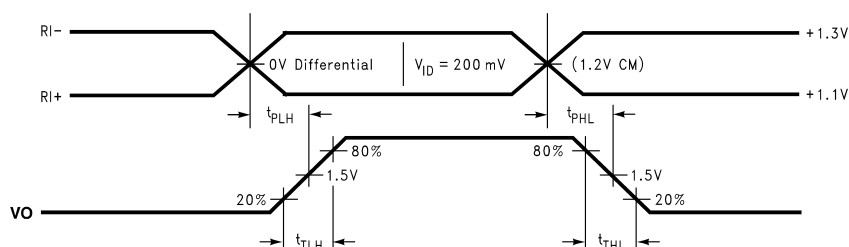


Figure 9. Receiver Propagation Delay and Transition Time Waveforms

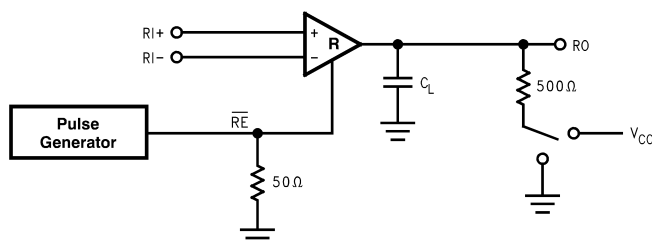


Figure 10. Receiver TRI-STATE Delay Test Circuit

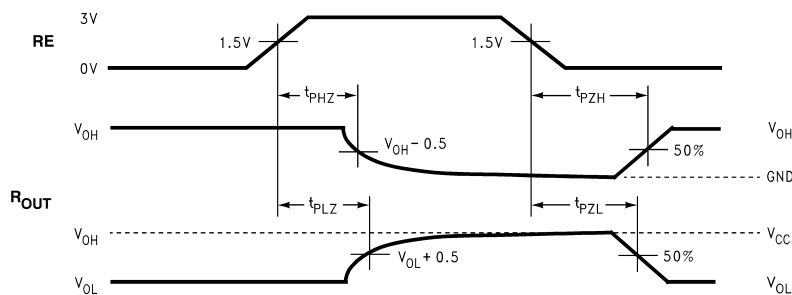


Figure 11. Receiver TRI-STATE Delay Waveforms TRI-STATE Delay Waveforms

TYPICAL BUS APPLICATION CONFIGURATIONS

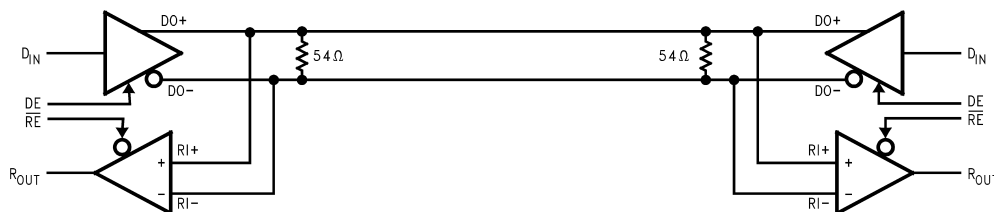


Figure 12. Bi-Directional Half-Duplex Point-to-Point Applications

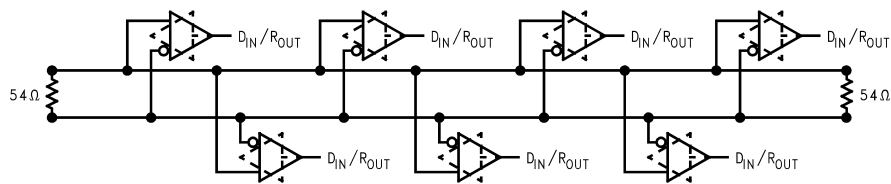


Figure 13. Multi-Point Bus Applications

APPLICATION INFORMATION

There are a few common practices which should be implied when designing PCB for BLVDS signaling. Recommended practices are:

- Use at least 4 layer PCB board (BLVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (BLVDS port side) connector as possible.
- Bypass each BLVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best. Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1 μ F, and 0.01 μ F in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused LVDS receiver inputs open (floating)

Table 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

Table 2. Transmitter Mode⁽¹⁾

INPUTS		OUTPUTS	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	$2 > \& > 0.8$	X	X
L	X	Z	Z

(1) L = Low state
H = High state

Table 3. Receiver Mode⁽¹⁾

INPUTS		OUTPUT
$\overline{RE}$	(RI+)-(RI-)	
L	L (< -100 mV)	L
L	H (> +100 mV)	H
L	$100 \text{ mV} > \& > -100 \text{ mV}$	X
H	X	Z

(1) X = High or Low logic state
Z = High impedance state
L = Low state
H = High state

Table 4. Device Pin Descriptions

Pin Name	Pin No.	Input/Output	Description
DIN	2	I	TTL Driver Input
DO $\pm$ /RI $\pm$	6, 7	I/O	LVDS Driver Outputs/LVDS Receiver Inputs
R _{OUT}	3	O	TTL Receiver Output
$\overline{RE}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V _{CC}	8	NA	Power Supply

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS92LV010ATM/NOPB	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV010 ATM
DS92LV010ATM/NOPB.A	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV010 ATM
DS92LV010ATMX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV010 ATM
DS92LV010ATMX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV010 ATM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

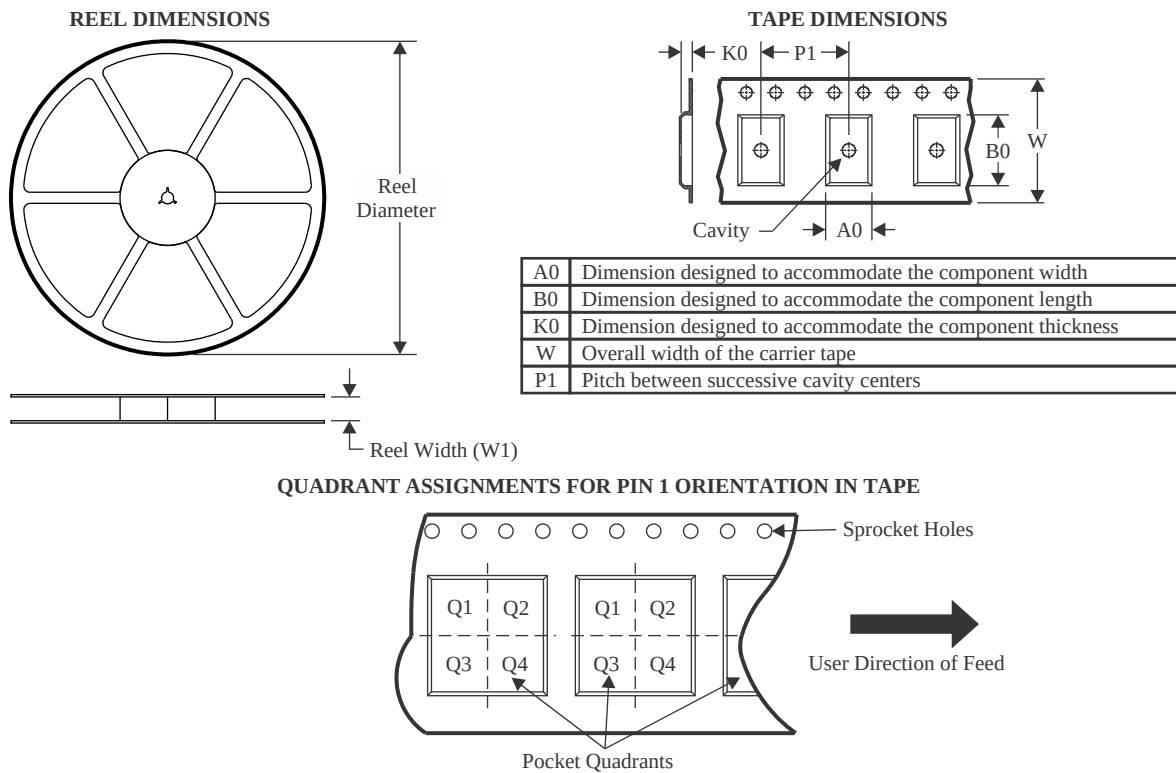
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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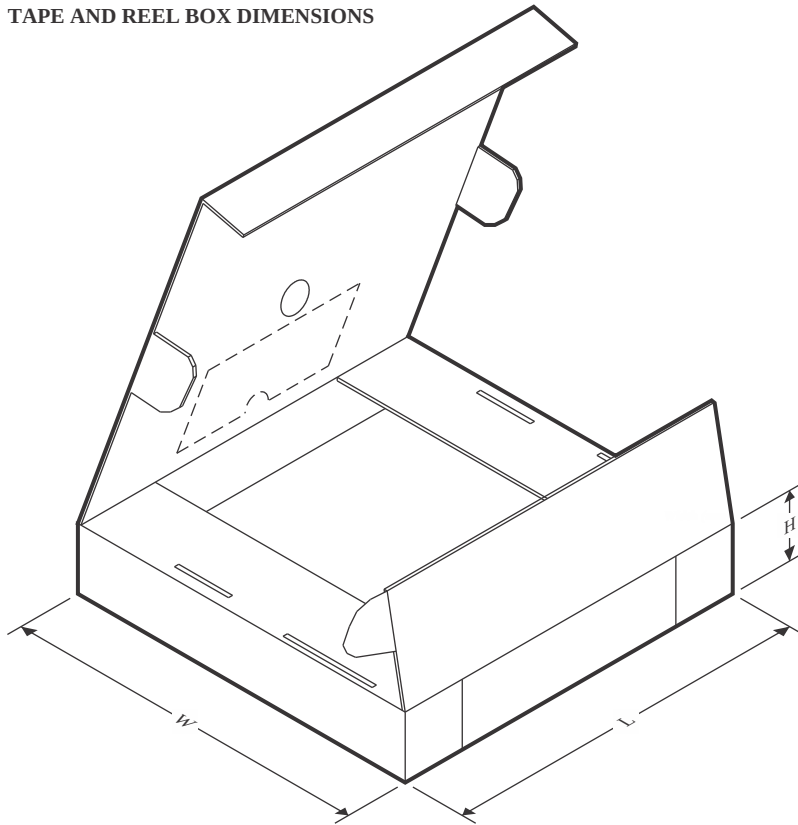
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV010ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

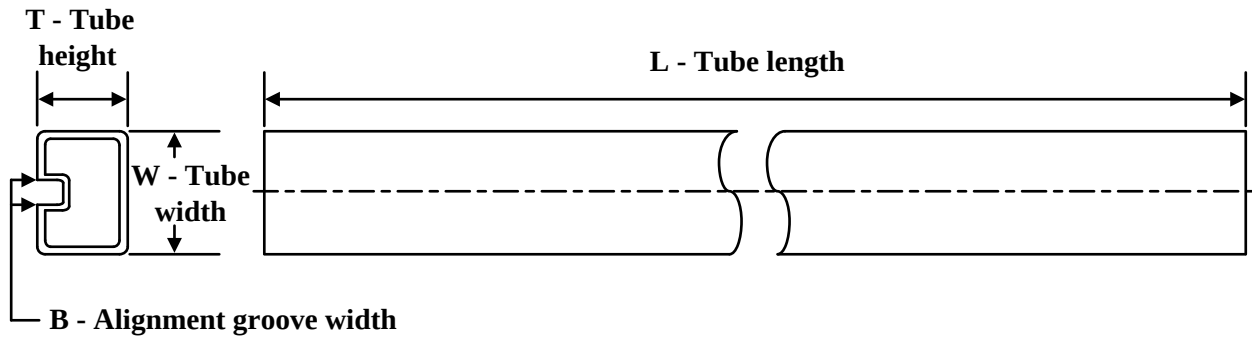
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

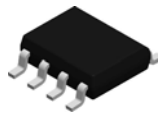
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV010ATMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS92LV010ATM/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS92LV010ATM/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

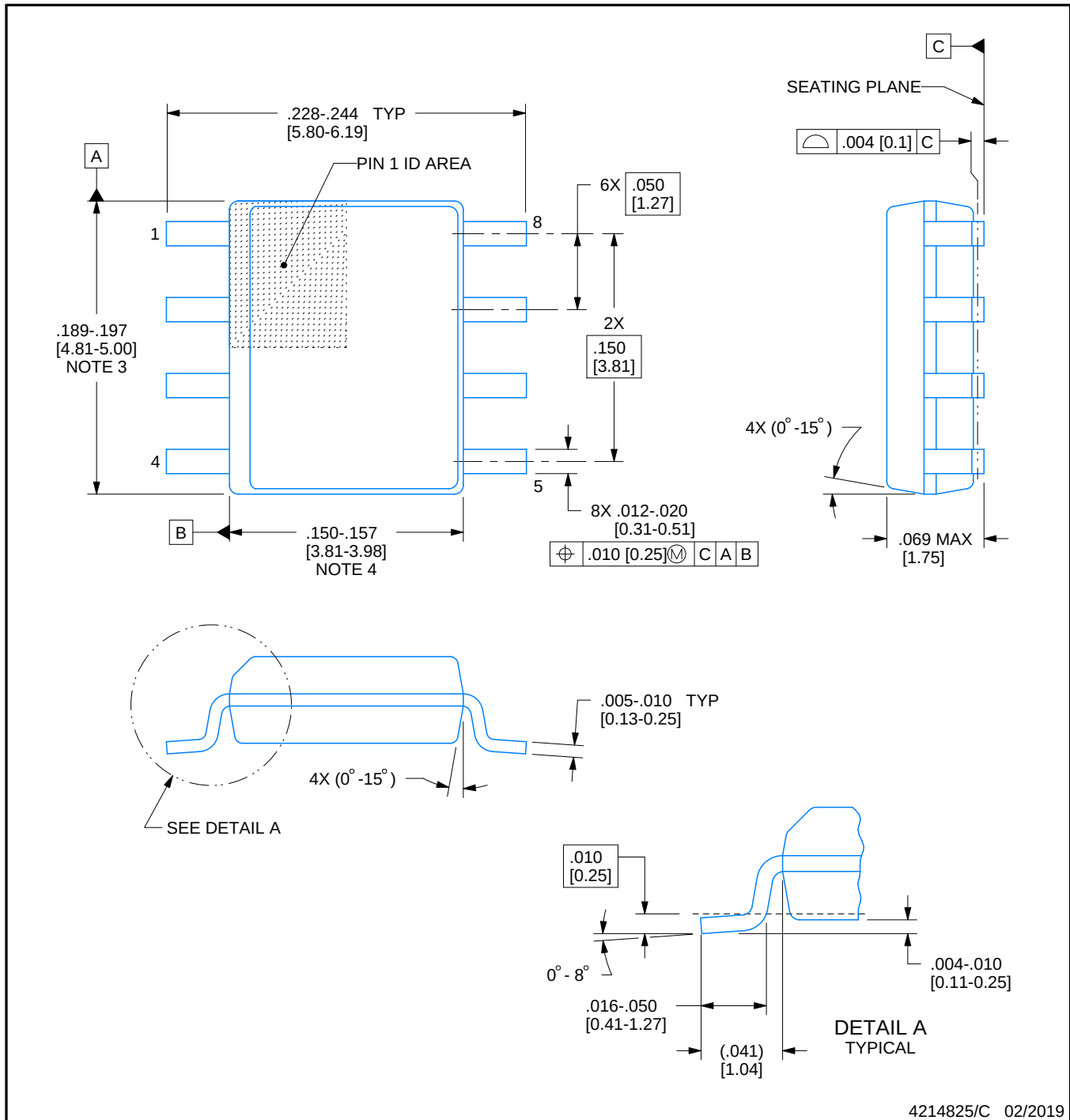


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

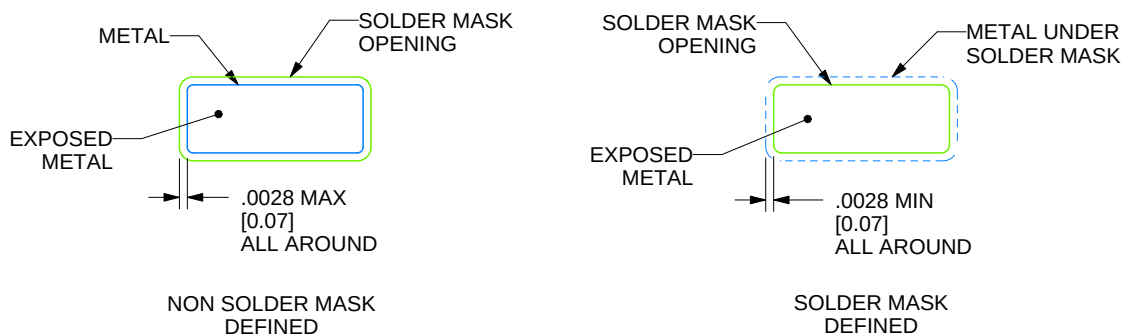
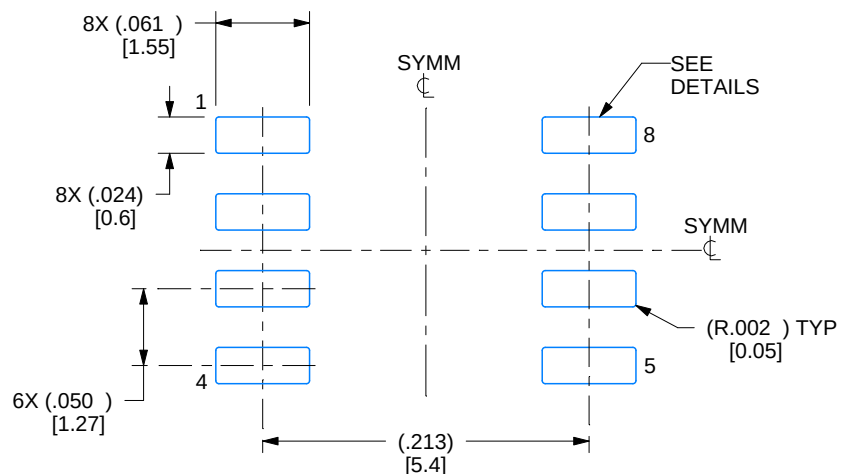
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

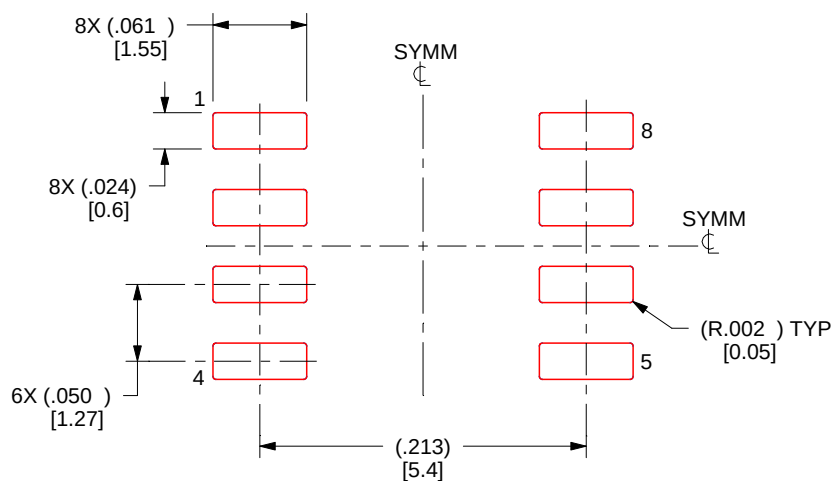
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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