

SNx5LBC179A Low-Power Differential Line Driver and Receiver Pairs

1 Features

- High-speed low-power LinBiCMOS™ circuitry designed for signaling rates⁽¹⁾ of up to 30 Mbps
- Bus-pin ESD protection exceeds 12 kV HBM
- Very low disabled supply-current requirements: 700 μ A Max
- Common-mode voltage range of -7 V to 12 V
- Low supply current: 15 mA Max
- Compatible with ANSI standard TIA/EIA-485-A and ISO8482: 1987(E)
- Positive and negative output current limiting
- Driver thermal shutdown protection ¹

2 Description

The SN65LBC179A and SN75LBC179A differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that are compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E). The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

The SN65LBC179A and SN75LBC179A combine a differential line driver and differential input line receiver and operate from a single 5-V supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off ($V_{CC} = 0$). These parts feature a wide positive and negative common-mode voltage range making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions.

The SN65LBC179A is characterized over the industrial temperature range of -40°C to 85°C . The SN75LBC179A is characterized for operation over the commercial temperature range of 0°C to 70°C .

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN65LBC179ASN75LBC179A	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

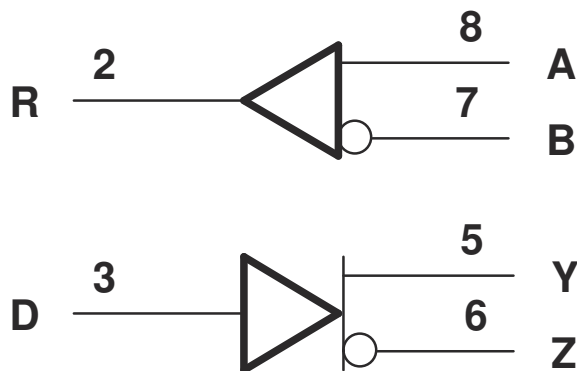


Figure 2-1. Logic Diagram (Positive Logic)

¹ (1) Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit length, and much higher signaling rates may be achieved without this requirement as displayed in the *TYPICAL CHARACTERISTICS* of this device.



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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2011) to Revision E (January 2023)	Page
• Changed the document to the latest TI format.....	1
• Added the <i>Thermal Information</i> table.....	5
• Changed the <i>Typical Characteristics</i> graphs.....	7

Changes from Revision C (June 2001) to Revision D (September 2011)	Page
• Added Receiver output current to the Abs Max Table	4
• Changed ESD - All terminals, Class 3, A From: 4 kV To: 3 kV.....	4
• Changed the D Output and R Output schematics.....	12

4 Pin Configuration and Functions

SN65LBC179AD (Marked as BL179A)
SN65LBC179AP (Marked as 65LBC179A)
SN75LBC179AD (Marked as LB179A)
SN75LBC179AP (Marked as 75LBC179A)
(TOP VIEW)

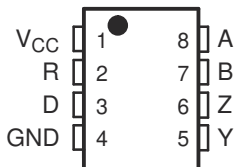


Table 4-1. Pin Functions

NO	Name	Type	Description
1	V _{CC}	Supply	4.75V to 5.25V Supply
2	R	O	Receive data output
3	D	I	Driver data input
4	GND	GND	Device ground
5	Y	O	Digital bus output, Y (Complementary to Z)
6	Z	O	Digital bus output, Z (Complementary to Y)
7	B	I	Bus input, B (complementary to A)
8	A	I	Bus input, A (complementary to B)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.3 V to 6 V
	Voltage range	A, B, Y, or Z ⁽²⁾	−10 V to 15 V
		D or R ⁽²⁾	−0.3 V to V _{CC} + 0.5 V
I _O	Receiver output current		±20 mA
	Electrostatic discharge	Bus terminals and GND, Class 3, A ⁽³⁾	12 kV
		Bus terminals and GND, Class 3, B ⁽³⁾	400 V
		All terminals, Class 3, A	3 kV
		All terminals, Class 3, B	400 V
Continuous total power dissipation ⁽⁴⁾			Internally limited
Total power dissipation			See Dissipation Rating Table

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to GND.
- (3) Tested in accordance with MIL-STD-883C, Method 3015.7
- (4) The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

5.2 Dissipation Ratings

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1100 mW	8.08 mW/°C	640 mW	520 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5	5.25	V
V _{IH}	High-level input voltage	D	2		V _{CC}	V
V _{IL}	Low-level input voltage	D	0		0.8	V
V _{ID}	Differential input voltage ⁽¹⁾		–12 ⁽²⁾		12	V
V _O	Voltage at any bus terminal (separately or common-mode)	A, B, Y, or Z	–7		12	V
V _I						
V _{IC}						
I _{OH}	High-level output current	Y or Z	–60			mA
		R	–8			
I _{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T _A	Operating free-air temperature	SN65LBC179A	–40		85	°C
		SN75LBC179A	0		70	

- (1) Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.
- (2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		P (PDIP)	D (SOIC) SN65 Device	D (SOIC) SN75 Device	UNIT
		8-Pins	8-Pins	8-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.7	116.7	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	54.7	56.3	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	63.4	53.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23	8.8	4.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.7	62.2	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-1.5	-0.8		V
$ V_{OD} $	Differential output voltage	$R_L = 54 \Omega$, See Figure 6-1	SN65LBC179A	1	1.5	3	V
			SN75LBC179A	1.1	1.5	3	
		$R_L = 60 \Omega$, $-7 < V_{(tot)} < 12$, See Figure 6-2	SN65LBC179A	1	1.5	3	V
			SN75LBC179A	1.1	1.5	3	
$\Delta V_{OD} $	Change in magnitude of differential output voltage ⁽²⁾	See Figure 6-1 and Figure 6-2		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 6-1		1.8	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage ⁽²⁾			-0.1		0.1	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7 \text{ V to } 12 \text{ V}$	-10	± 1	10	μA
I_{IH}	High-level input current	$V_I = 2. \text{V}$		-100			μA
I_{IL}	Low-level input current	$V_I = 0.8 \text{ V}$		-100			μA
I_{OS}	Short-circuit output current	$-7 \text{ V} \leq V_O \leq 12 \text{ V}$		-250	± 70	250	mA
I_{CC}	Supply current	No load,	$V_I = 0 \text{ or } V_{CC}$		8.5	15	mA

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

5.6 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 54\ \Omega$, $C_L = 50\ \text{pF}$, See Figure 6-3	2	6	12	ns
t_{PHL} Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$ Pulse skew ($ t_{PHL} - t_{PLH} $)			0.3	1	ns
t_r Differential output signal rise time		4	7.5	11	ns
t_f Differential output signal fall time		4	7.5	11	ns

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$I_O = -8\ \text{mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$I_O = 8\ \text{mA}$	-0.2			
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_{OH} High-level output voltage	$V_{ID} = 200\ \text{mV}$, $I_{OH} = -8\ \text{mA}$, See Figure 6-1	4	4.9		V
V_{OL} Low-level output voltage	$V_{ID} = -200\ \text{mV}$, $I_{OL} = 8\ \text{mA}$, See Figure 6-1		0.1	0.8	V
I_I Bus input current	$V_{IH} = 12\ \text{V}$, $V_{CC} = 5\ \text{V}$	Other input at 0 V	0.4	1	mA
	$V_{IH} = 12\ \text{V}$, $V_{CC} = 0$		0.5	1	
	$V_{IH} = -7\ \text{V}$, $V_{CC} = 5\ \text{V}$		-0.8	-0.4	
	$V_{IH} = -7\ \text{V}$, $V_{CC} = 0$		-0.8	-0.3	

5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$V_{ID} = -1.5\ \text{V}$ to $1.5\ \text{V}$, See Figure 6-4	7	13	20	ns
t_{PHL} Propagation delay time, high-to-low-level output		7	13	20	ns
$t_{sk(p)}$ Pulse skew ($ t_{PLH} - t_{PHL} $)			0.5	1.5	ns
t_r Rise time, output			2.1	3.3	ns
t_f Fall time, output	See Figure 6-4		2.1	3.3	ns

5.9 Typical Characteristics

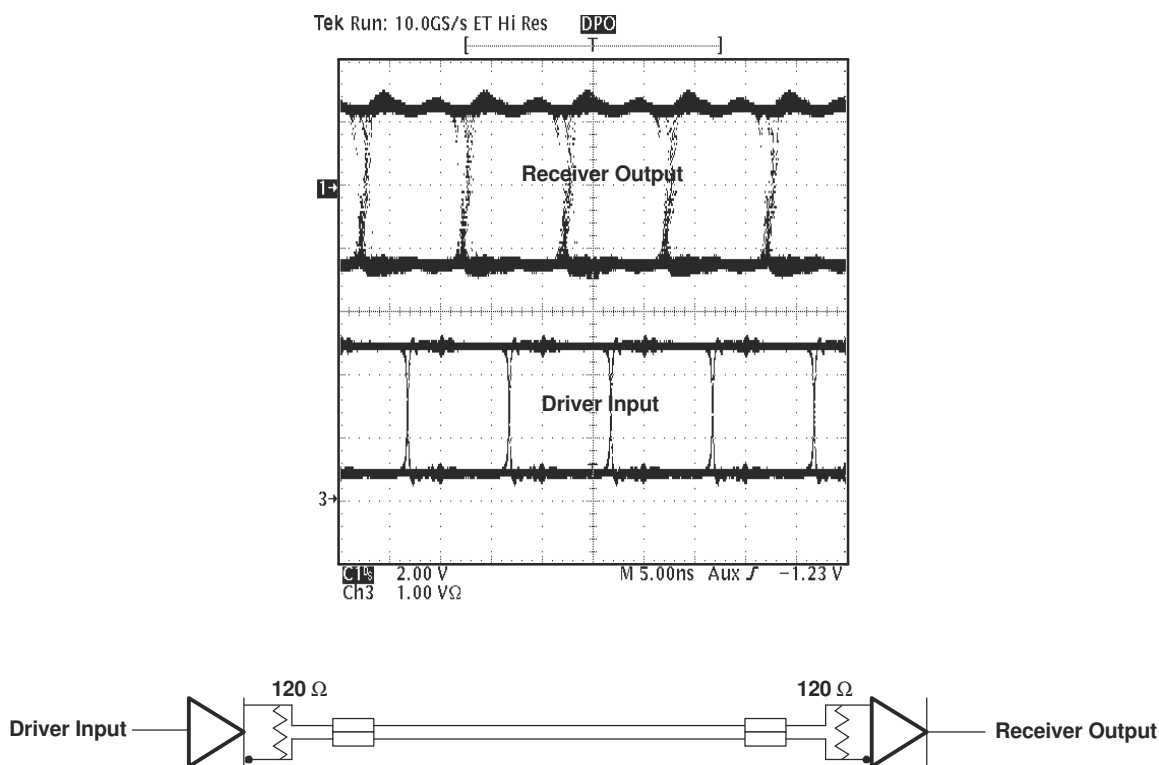


Figure 5-1. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

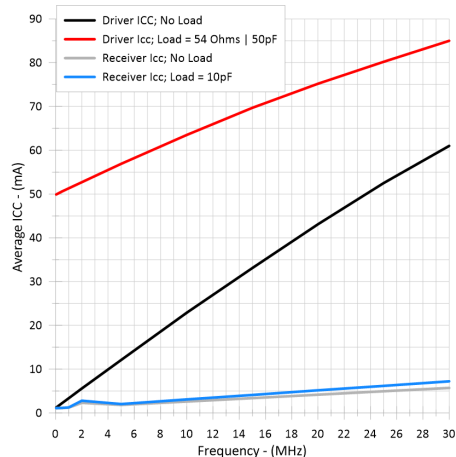


Figure 5-2. Average Supply Current vs Frequency

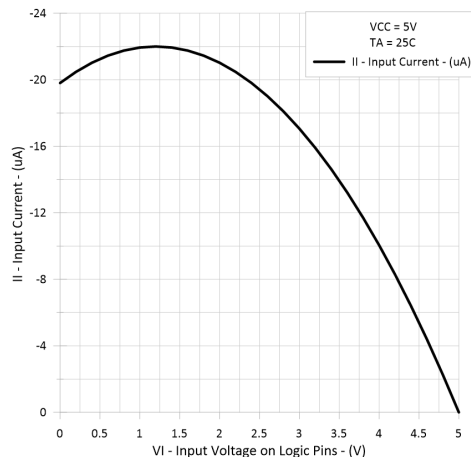


Figure 5-3. Logic Input Current vs Input Voltage

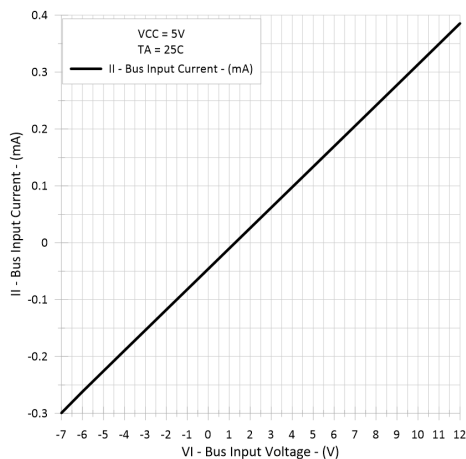


Figure 5-4. Input Current vs Input Voltage

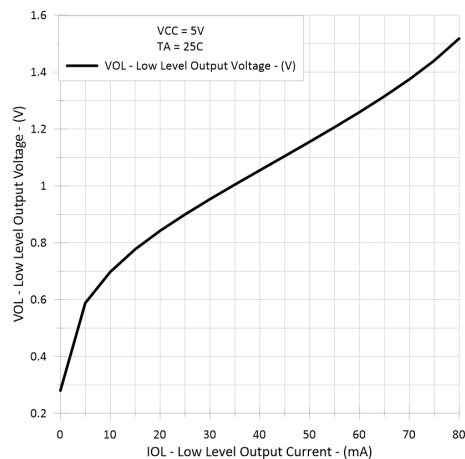


Figure 5-5. Low-Level Output Voltage vs Low-Level Output Current

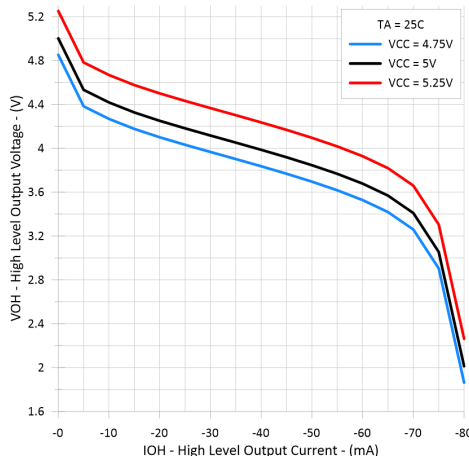


Figure 5-6. Driver High-Level Output Voltage vs HIGH-Level Output Current

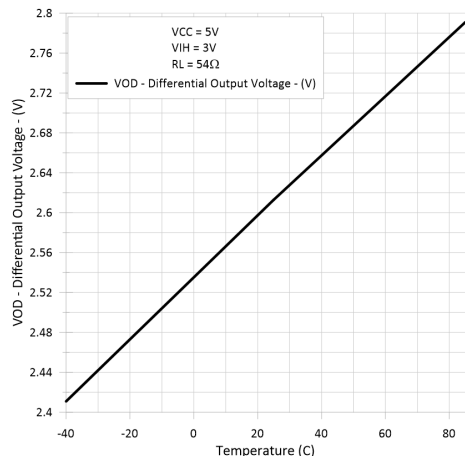


Figure 5-7. Driver Differential Output Voltage vs Average Case Temperature

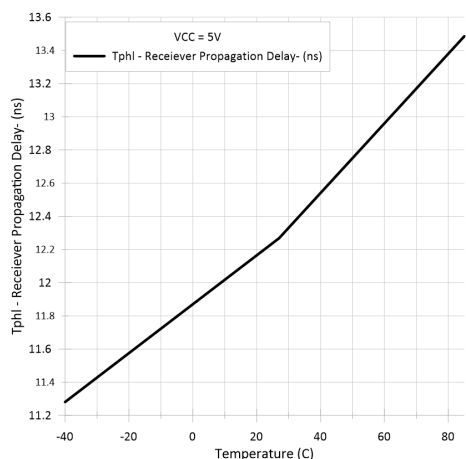


Figure 5-8. Receiver Propagation Time vs Case Temperature

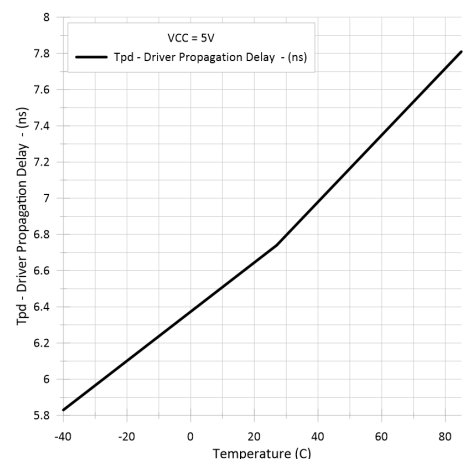


Figure 5-9. Driver Propagation Delay Time vs Case Temperature

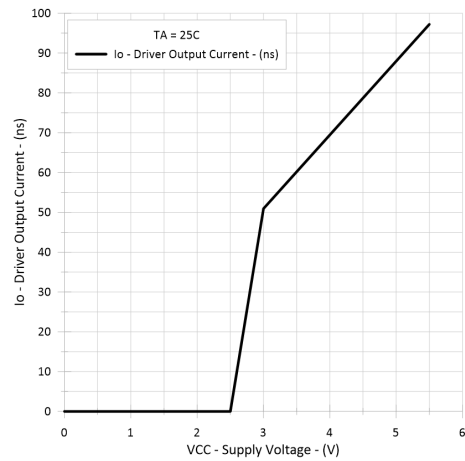


Figure 5-10. Driver Output Current vs Supply Voltage

6 Parameter Measurement Information

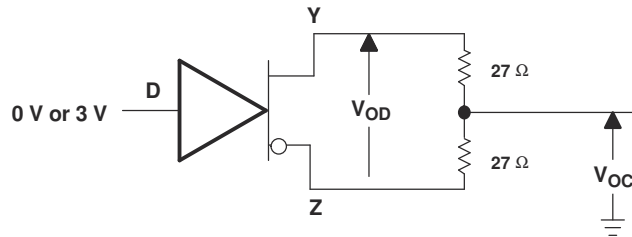


Figure 6-1. Driver V_{OD} and V_{OC}

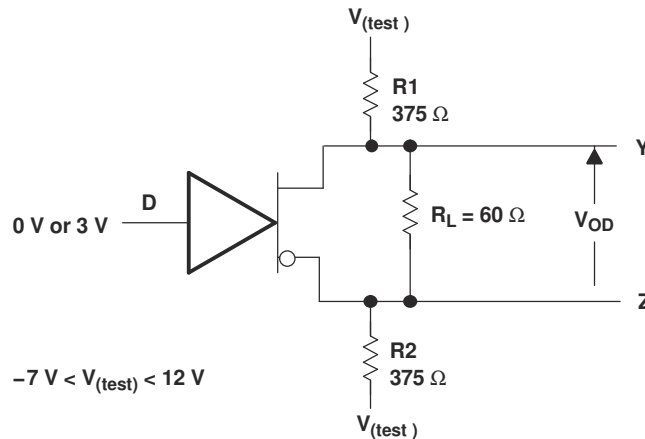
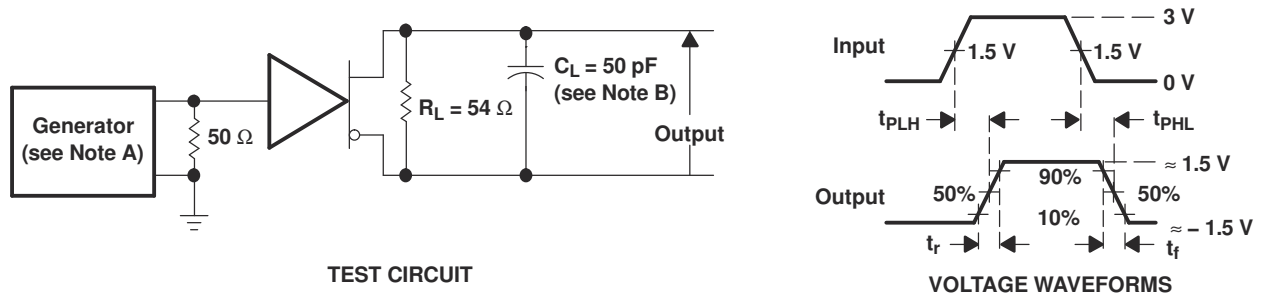
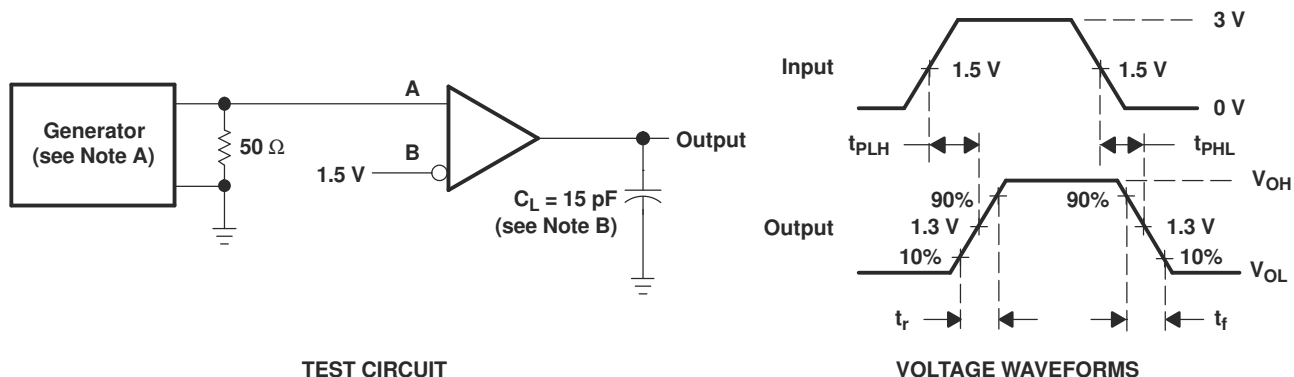


Figure 6-2. Driver V_{OD} With Common-Mode Loading



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 6-3. Driver Test Circuits and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 6-4. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

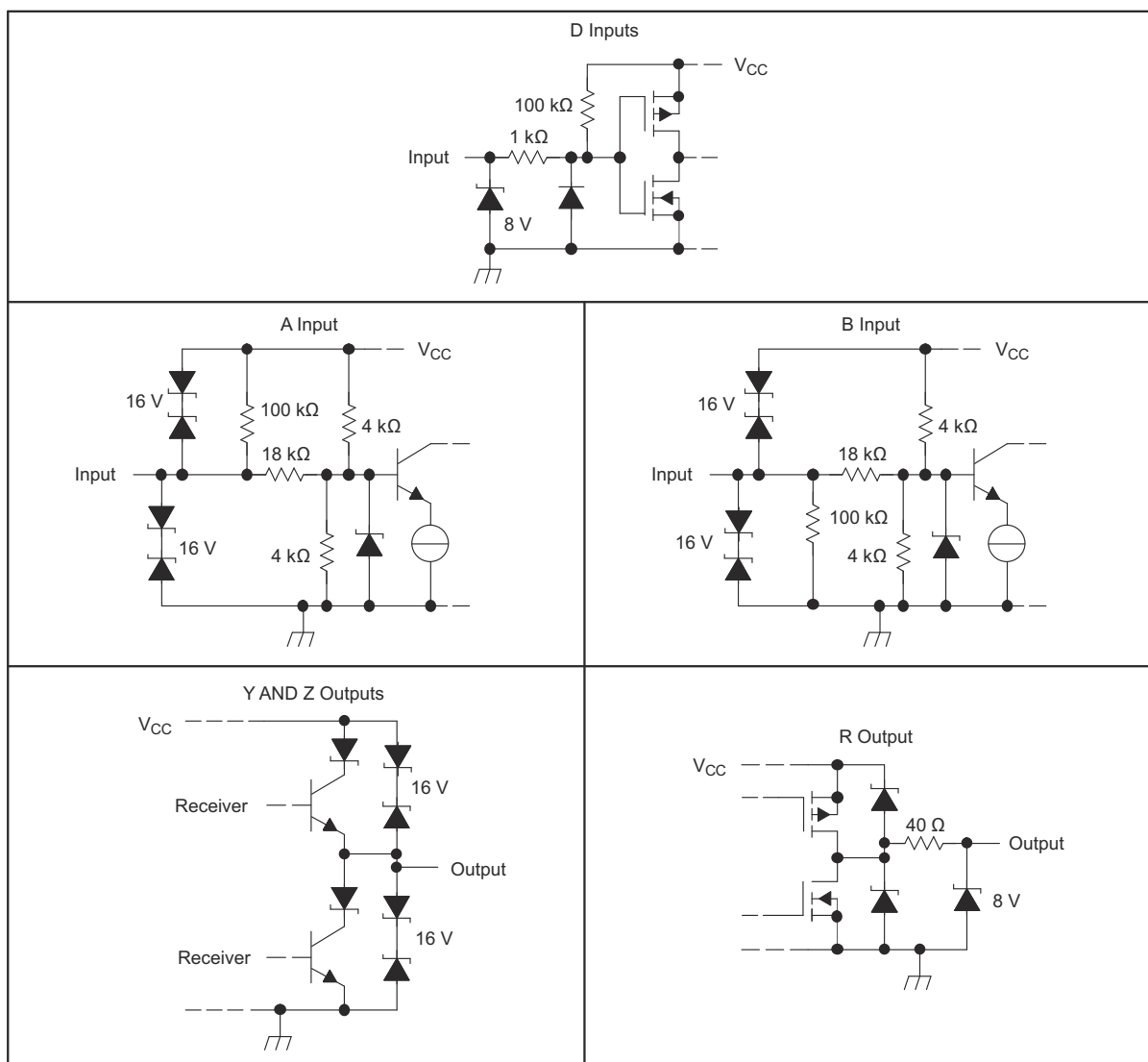
7.1.1 FUNCTION TABLE

DRIVER			RECEIVER	
INPUT D	OUTPUTS ⁽¹⁾		DIFFERENTIAL INPUTS A – B	OUTPUT R
	Y	Z		
			$V_{ID} \geq 0.2 \text{ V}$	H
H	H	L	$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	?
L	L	H	$V_{ID} \leq -0.2 \text{ V}$	L
OPEN	H	L	Open circuit	H

(1) H = high level, L = low level, ? = indeterminate

7.1.2 Schematics

Schematics of Inputs and Output



8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC179ADR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A
SN65LBC179ADR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A
SN65LBC179ADRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL179A
SN65LBC179AP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC179A
SN65LBC179AP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC179A
SN75LBC179ADR	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	LB179A
SN75LBC179AP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC179A
SN75LBC179AP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC179A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

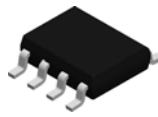
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179ADR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC179AP	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC179AP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC179AP	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC179AP.A	P	PDIP	8	50	506	13.97	11230	4.32

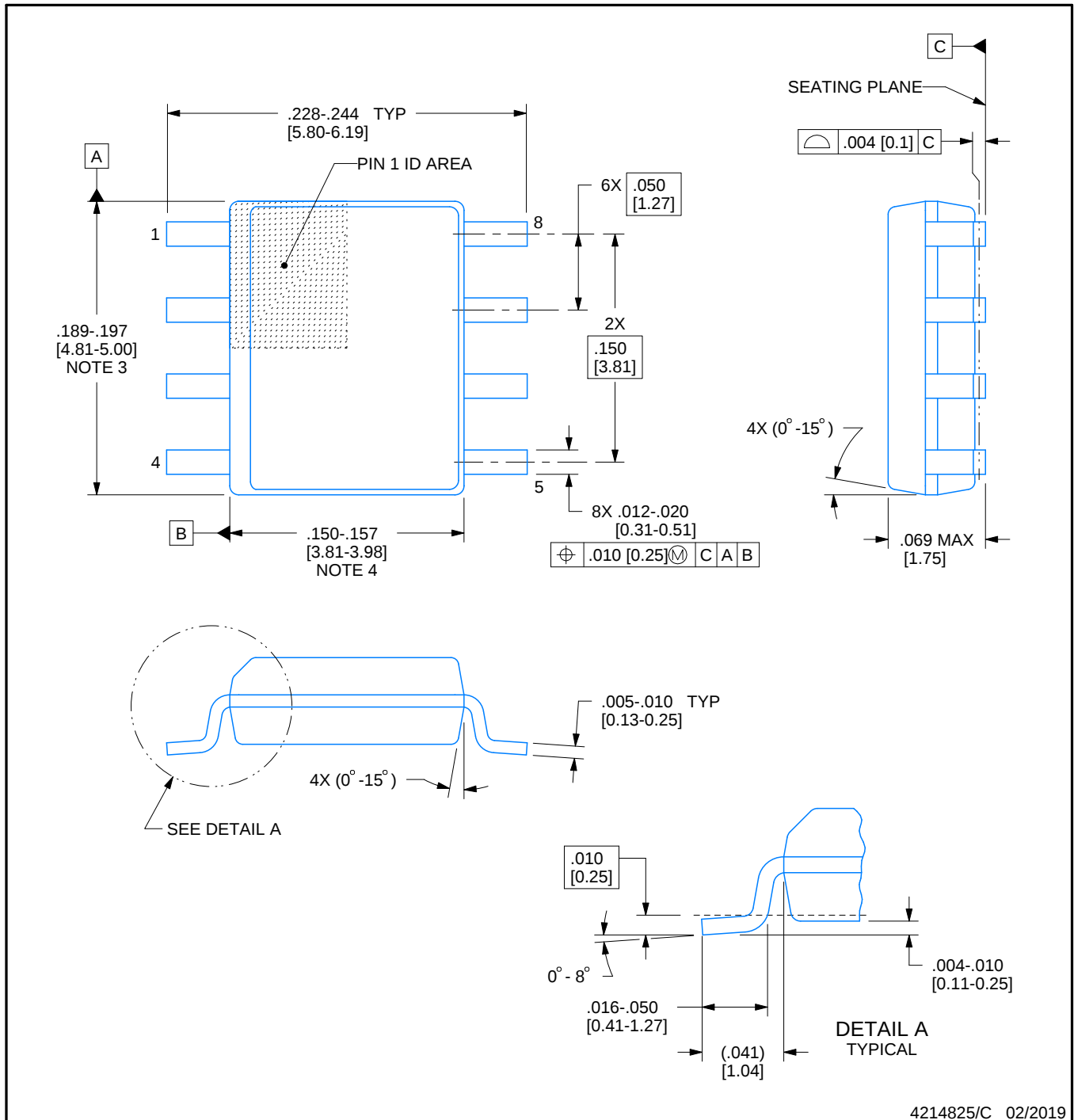


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

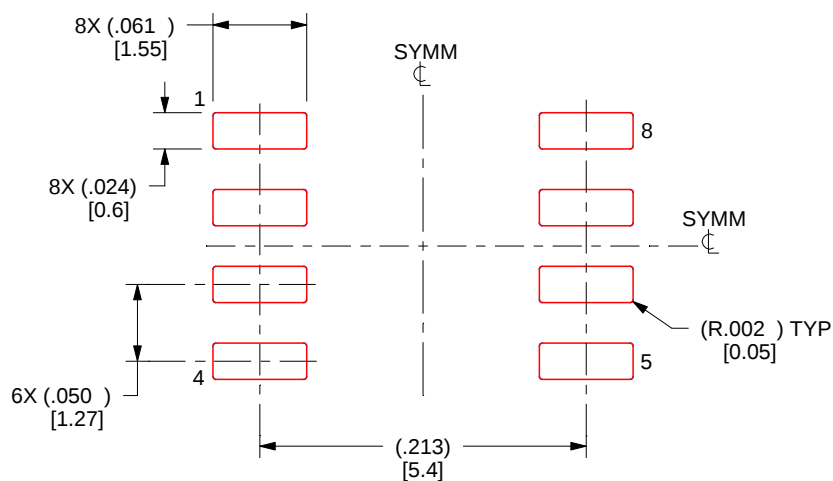
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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