

# GD65232, GD75232 Multiple RS-232 Drivers and Receivers

## 1 Features

- Single chip with easy interface between UART and serial-port connector of IBM PC/AT and compatibles
- Meet or exceed the requirements of TIA/EIA-232-F and ITU v.28 standards
- Designed to support data rates up to 120kbits
- Pinout compatible with SN75C185 and SN75185
- ESD performance tested per JESD 22: HBM; 1500V, CDM: 500V, MM; 200V

## 2 Applications

- Terminals
- [Modems](#)
- Computers
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Hand-held equipment](#)

## 3 Description

The GD65232 and GD75232 combine three drivers and five receivers from the Texas Instruments trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™ PC/AT and compatibles. The bipolar circuits and processing of the GD65232 and GD75232 provide a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

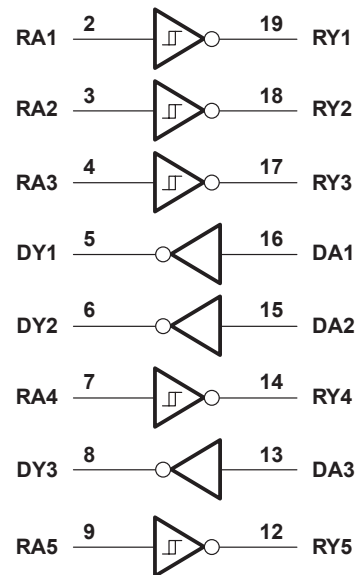
The GD65232 and GD75232 comply with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20kbits. The switching speeds of these devices are fast enough to support rates up to 120kbits with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120kbits, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

### Package Information

| PART NUMBER        | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|--------------------|------------------------|-----------------------------|
| GD65232<br>GD75232 | SSOP (DB, 20)          | 7.2mm x 7.8mm               |
|                    | SOIC (DW, 20)          | 12.8mm x 10.3mm             |
|                    | PDIP (N, 20)           | 24.33mm x 9.4mm             |
|                    | TSSOP (PW, 20)         | 6.5mm x 6.4mm               |

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



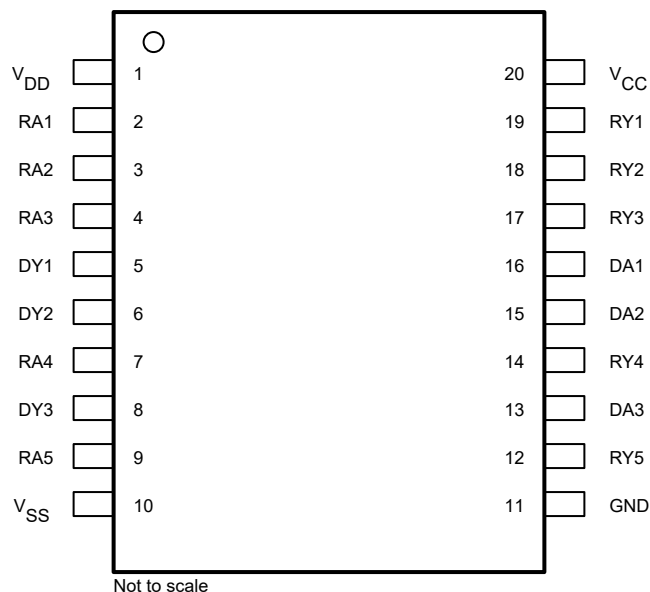
Logic Diagram (positive logic)



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## 4 Pin Configuration and Functions



**Figure 4-1. DB, DW, N, OR PW Package  
(Top View)**

**Table 4-1. Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                 |
|-----------------|-----|---------------------|-----------------------------|
| NAME            | NO. |                     |                             |
| V <sub>DD</sub> | 1   | –                   | Positive RS232 Power Supply |
| RA1             | 2   | I                   | RS232 Input                 |
| RA2             | 3   | I                   | RS232 Input                 |
| RA3             | 4   | I                   | RS232 Input                 |
| DY1             | 5   | O                   | RS232 Output                |
| DY2             | 6   | O                   | RS232 Output                |
| RA4             | 7   | I                   | RS232 Input                 |
| DY3             | 8   | O                   | RS232 Output                |
| RA5             | 9   | I                   | RS232 Input                 |
| V <sub>SS</sub> | 10  | –                   | Negative RS232 Power Supply |
| GND             | 11  | –                   | Ground                      |
| RY5             | 12  | O                   | TTL Output                  |
| DA3             | 13  | I                   | TTL Input                   |
| RY4             | 14  | O                   | TTL Output                  |
| DA2             | 15  | I                   | TTL Input                   |
| DA1             | 16  | I                   | TTL Input                   |
| RY3             | 17  | O                   | TTL Output                  |
| RY2             | 18  | O                   | TTL Output                  |
| RY1             | 19  | O                   | TTL Output                  |
| V <sub>CC</sub> | 20  | –                   | Device Power Supply for TTL |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                                        | MIN | MAX | UNIT |
|------------------|----------------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage (see <sup>(2)</sup> )   |     | 10  | V    |
| V <sub>DD</sub>  |                                        |     | 15  | V    |
| V <sub>SS</sub>  |                                        |     | –15 | V    |
| V <sub>I</sub>   | Input voltage range, Driver            | –15 | 7   | V    |
|                  | Input voltage range, Receiver          | –30 | 30  | V    |
| V <sub>O</sub>   | Driver output voltage range            | –15 | 15  | V    |
| I <sub>OL</sub>  | Receiver low-level output current      |     | 20  | mA   |
| T <sub>J</sub>   | Operating virtual junction temperature |     | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range              | –65 | 150 | °C   |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the network ground terminal

### 5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                        |          | MIN  | NOM | MAX  | UNIT |
|-----------------|----------------------------------------|----------|------|-----|------|------|
| V <sub>DD</sub> | Supply voltage (see <sup>(1)</sup> )   |          | 7.5  | 9   | 15   | V    |
| V <sub>SS</sub> | Supply voltage (see <sup>(1)</sup> )   |          | –7.5 | –9  | –15  | V    |
| V <sub>CC</sub> | Supply voltage (see <sup>(1)</sup> )   |          | 4.5  | 5   | 5.5  | V    |
| V <sub>IH</sub> | High-level input voltage (driver only) |          | 1.9  |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage (driver only)  |          |      |     | 0.8  | V    |
| I <sub>OH</sub> | High-level output current              | Driver   |      |     | –6   | mA   |
|                 |                                        | Receiver |      |     | –0.5 |      |
| I <sub>OL</sub> | Low-level output current               | Driver   |      |     | 6    | mA   |
|                 |                                        | Receiver |      |     | 16   |      |
| T <sub>A</sub>  | Operating free-air temperature         | GD65232  | –40  |     | 85   | °C   |
|                 |                                        | GD75232  | 0    |     | 70   |      |

(1) When powering up the GD65232 and GD75232, the following sequence should be used:

- V<sub>SS</sub>, V<sub>DD</sub>, V<sub>CC</sub>, I/Os

Applying V<sub>CC</sub> before V<sub>DD</sub> may allow large currents to flow, causing damage to the device. When powering down the GD65232 and GD75232, the reverse sequence should be used

## 5.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | DB<br>(SSOP) | DW<br>(SOIC) | N<br>(PDIP) | PW<br>(TSSOP) | UNIT |
|-------------------------------|----------------------------------------------|--------------|--------------|-------------|---------------|------|
|                               |                                              | 20 PINS      | 20 PINS      | 20 PINS     | 20 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 92.0         | 73.0         | 59.8        | 97.5          | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 54.3         | 40.2         | 39.1        | 41.3          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 57.0         | 45.7         | 36.1        | 59.2          | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 14.7         | 12.8         | 18.3        | 4.1           | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 56.3         | 45.0         | 35.7        | 58.6          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Supply Currents over Recommended Operating Free-air Temperature Range

over operating free-air temperature range (unless otherwise noted)

|                 | PARAMETER                           | TEST CONDITIONS    |                               |                       |                        | MIN | MAX  | UNIT |
|-----------------|-------------------------------------|--------------------|-------------------------------|-----------------------|------------------------|-----|------|------|
| I <sub>DD</sub> | Supply current from V <sub>DD</sub> | All inputs at 1.9V | No load                       | V <sub>DD</sub> = 9V  | V <sub>SS</sub> = -9V  |     | 15   | mA   |
|                 |                                     |                    |                               | V <sub>DD</sub> = 12V | V <sub>SS</sub> = -12V |     | 19   |      |
|                 |                                     |                    |                               | V <sub>DD</sub> = 15V | V <sub>SS</sub> = -15V |     | 25   |      |
|                 |                                     | All inputs at 0.8V | No load                       | V <sub>DD</sub> = 9V  | V <sub>SS</sub> = -9V  |     | 4.5  |      |
|                 |                                     |                    |                               | V <sub>DD</sub> = 12V | V <sub>SS</sub> = -12V |     | 5.5  |      |
|                 |                                     |                    |                               | V <sub>DD</sub> = 15V | V <sub>SS</sub> = -15V |     | 9    |      |
| I <sub>SS</sub> | Supply current from V <sub>SS</sub> | All inputs at 1.9V | No load                       | V <sub>DD</sub> = 9V  | V <sub>SS</sub> = -9V  |     | -15  | mA   |
|                 |                                     |                    |                               | V <sub>DD</sub> = 12V | V <sub>SS</sub> = -12V |     | -19  |      |
|                 |                                     |                    |                               | V <sub>DD</sub> = 15V | V <sub>SS</sub> = -15V |     | -25  |      |
|                 |                                     | All inputs at 0.8V | No load                       | V <sub>DD</sub> = 9V  | V <sub>SS</sub> = -9V  |     | -3.2 |      |
|                 |                                     |                    |                               | V <sub>DD</sub> = 12V | V <sub>SS</sub> = -12V |     | -3.2 |      |
|                 |                                     |                    |                               | V <sub>DD</sub> = 15V | V <sub>SS</sub> = -15V |     | -3.2 |      |
| I <sub>CC</sub> | Supply current from V <sub>CC</sub> | All inputs at 5V   | No load, V <sub>CC</sub> = 5V | GD65232               |                        |     | 38   | mA   |
|                 |                                     |                    |                               | GD75232               |                        |     | 30   |      |

## 5.5 Electrical Characteristics, Driver

over operating free-air temperature range  $V_{DD} = 9V$ ,  $V_{SS} = -9V$ ,  $V_{CC} = 5V$  (unless otherwise noted)

|             | PARAMETER                                         | TEST CONDITIONS                  |                     |                | MIN  | TYP  | MAX   | UNIT     |
|-------------|---------------------------------------------------|----------------------------------|---------------------|----------------|------|------|-------|----------|
| $V_{OH}$    | High-level output voltage                         | $V_{IL} = 0.8V$ ,                | $R_L = 3k\Omega$ ,  | See Figure 6-1 | 6    | 7.5  |       | V        |
| $V_{OL}$    | Low-level output voltage (see (1))                | $V_{IH} = 1.9V$ ,                | $R_L = 3k\Omega$ ,  | See Figure 6-1 |      | -7.5 | -6    | V        |
| $I_{IH}$    | High-level input current                          | $V_I = 5V$ ,                     | See Figure 6-2      |                |      |      | 10    | $\mu A$  |
| $I_{IL}$    | Low-level input current                           | $V_I = 0$ ,                      | See Figure 6-2      |                |      |      | -1.6  | mA       |
| $I_{OS(H)}$ | High-level short-circuit output current (see (2)) | $V_{IL} = 0.8V$ ,                | $V_O = 0$ ,         | See Figure 1   | -4.5 | -12  | -19.5 | mA       |
| $I_{OS(L)}$ | Low-level short-circuit output current            | $V_{IH} = 2V$ ,                  | $V_O = 0$ ,         | See Figure 6-1 | 4.5  | 12   | 19.5  | mA       |
| $r_o$       | Output resistance (see (3))                       | $V_{CC} = V_{DD} = V_{SS} = 0$ , | $V_O = -2V$ to $2V$ |                | 300  |      |       | $\Omega$ |

- (1) The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (that is, if -10V is maximum, the typical value is a more negative voltage).
- (2) Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings,
- (3) Test conditions are those specified by TIA/EIA-232-F and as listed above

## 5.6 Switching Characteristics, Driver

over operating free-air temperature range  $V_{CC} = 5V$ ,  $V_{DD} = 12V$ ,  $V_{SS} = -12V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

|           | PARAMETER                                         |                                  | TEST CONDITIONS                         | MIN | TYP | MAX | UNIT    |
|-----------|---------------------------------------------------|----------------------------------|-----------------------------------------|-----|-----|-----|---------|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $R_L = 3k\Omega$ to $7k\Omega$ , | $C_L = 15pF$ , See Figure 6-3           |     | 315 | 500 | ns      |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | $R_L = 3k\Omega$ to $7k\Omega$ , | $C_L = 15pF$ , See Figure 6-3           |     | 75  | 175 | ns      |
| $t_{TLH}$ | Transition time, low- to high-level output        | $R_L = 3k\Omega$ to $7k\Omega$   | $C_L = 15pF$ , See Figure 6-3           |     | 60  | 100 | ns      |
|           |                                                   |                                  | $C = 2500pF$ , See Figure 6-3 and (1)   |     | 1.7 | 2.5 | $\mu s$ |
| $t_{THL}$ | Transition time, high- to low-level output        | $R_L = 3k\Omega$ to $7k\Omega$   | $C_L = 15pF$ , See Figure 6-3           |     | 40  | 75  | ns      |
|           |                                                   |                                  | $C_L = 2500pF$ , See Figure 6-3 and (1) |     | 1.5 | 2.5 | $\mu s$ |

- (1) Measured between  $\pm 3V$  and  $\pm 3V$  points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

## 5.7 Electrical Characteristics, Receiver

over operating free-air temperature range (unless otherwise noted)

|                  | PARAMETER                                                       | TEST CONDITIONS                                              | MIN     | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|-----------------------------------------------------------------|--------------------------------------------------------------|---------|--------------------|------|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage                          | T <sub>A</sub> = 25°C, See <a href="#">Figure 6-5</a>        | 1.75    | 1.9                | 2.3  | V    |
|                  |                                                                 | T <sub>A</sub> = 0°C to 70°C, See <a href="#">Figure 6-5</a> | 1.55    |                    | 2.3  |      |
| V <sub>IT-</sub> | Negative-going input threshold voltage                          |                                                              | 0.75    | 0.97               | 1.25 | V    |
| V <sub>hys</sub> | Input hysteresis voltage (V <sub>IT+</sub> – V <sub>IT-</sub> ) |                                                              | 0.5     |                    |      | V    |
| V <sub>OH</sub>  | High-level output voltage                                       | I <sub>OH</sub> = –0.5mA                                     | 2.6     | 4                  | 5    | V    |
|                  |                                                                 | V <sub>IH</sub> = 0.75V<br>Inputs open                       | 2.6     |                    |      |      |
| V <sub>OL</sub>  | Low-level output voltage                                        | I <sub>OL</sub> = 10mA, V <sub>I</sub> = 3V                  |         | 0.2                | 0.45 | V    |
| I <sub>IH</sub>  | High-level input current                                        | V <sub>I</sub> = 25V, See <a href="#">Figure 6-5</a>         | GD65232 | 3.6                | 11   | mA   |
|                  |                                                                 |                                                              | GD75232 | 3.6                | 8.3  |      |
|                  |                                                                 | V <sub>I</sub> = 3V, See <a href="#">Figure 6-5</a>          |         | 0.43               |      |      |
| I <sub>IL</sub>  | Low-level input current                                         | V <sub>I</sub> = –25V, <a href="#">Figure 6-5</a>            | GD65232 | –3.6               | –11  | mA   |
|                  |                                                                 |                                                              | GD75232 | –3.6               | –8.3 |      |
|                  |                                                                 | V <sub>I</sub> = –3V, See <a href="#">Figure 6-5</a>         |         | –0.43              |      |      |
| I <sub>OS</sub>  | Short-circuit output current                                    | See <a href="#">Figure 6-4</a>                               |         | –3.4               | –12  | mA   |

(1) All typical values are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V, V<sub>DD</sub> = 9 V, and V<sub>SS</sub> = –9 V.

## 5.8 Switching Characteristics, Receiver

over operating free-air temperature range V<sub>CC</sub> = 5V, V<sub>DD</sub> = 12V, V<sub>SS</sub> = –12V, T<sub>A</sub> = 25°C (unless otherwise noted)

|                  | PARAMETER                                         | TEST CONDITIONS                                                               | MIN | TYP | MAX | UNIT |
|------------------|---------------------------------------------------|-------------------------------------------------------------------------------|-----|-----|-----|------|
| t <sub>PLH</sub> | Propagation delay time, low- to high-level output | C <sub>L</sub> = 50pF, R <sub>L</sub> = 5kΩ, See <a href="#">Figure 6-6</a>   |     | 107 | 250 | ns   |
| t <sub>PHL</sub> | Propagation delay time, high- to low-level output |                                                                               |     | 42  | 150 | ns   |
| t <sub>TLH</sub> | Transition time, low- to high-level output        |                                                                               |     | 175 | 350 | ns   |
| t <sub>THL</sub> | Transition time, high- to low-level output        |                                                                               |     | 16  | 60  | ns   |
| t <sub>PLH</sub> | Propagation delay time, low- to high-level output | C <sub>L</sub> = 15pF, R <sub>L</sub> = 1.5kΩ, See <a href="#">Figure 6-6</a> |     | 100 | 160 | ns   |
| t <sub>PHL</sub> | Propagation delay time, high- to low-level output |                                                                               |     | 60  | 100 | ns   |
| t <sub>TLH</sub> | Transition time, low- to high-level output        |                                                                               |     | 90  | 175 | ns   |
| t <sub>THL</sub> | Transition time, high- to low-level output        |                                                                               |     | 15  | 50  | ns   |

## 5.9 Typical Characteristics Driver

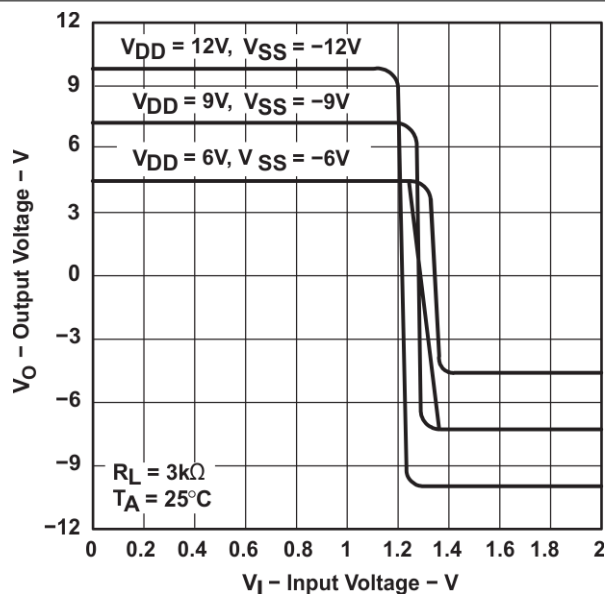


Figure 5-1. Voltage Transfer Characteristics

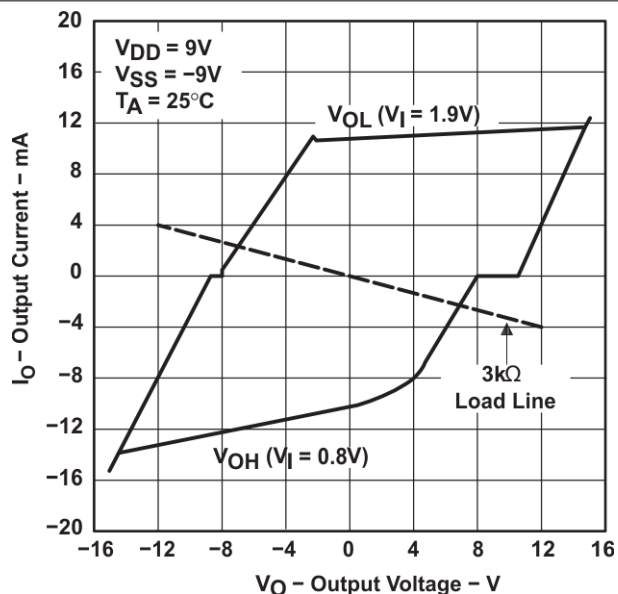


Figure 5-2. Output Current vs Output Voltage

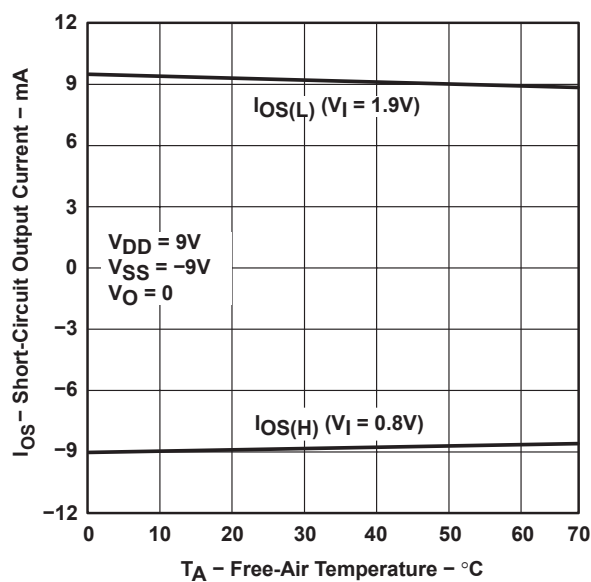


Figure 5-3. Short-Circuit Output Current vs Free-Air Temperature

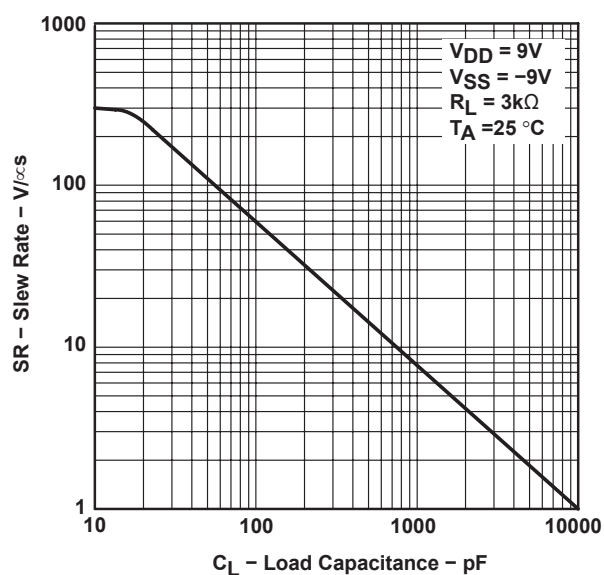


Figure 5-4. Slew Rate vs Load Capacitance



## 5.10 Typical Characteristics Receiver

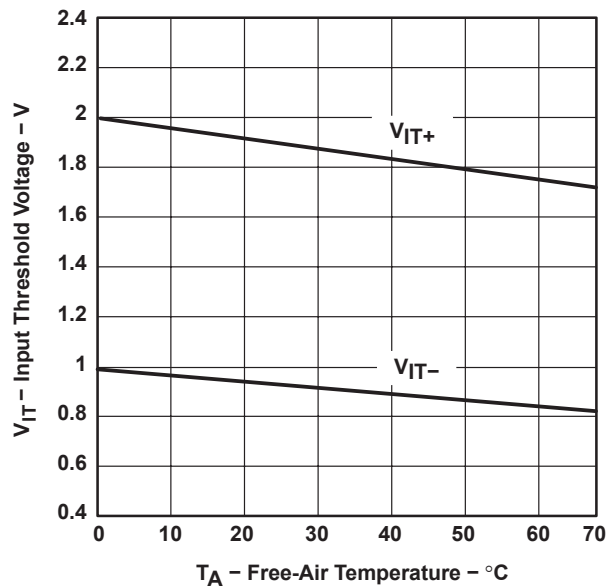


Figure 5-5. Input Threshold Voltage vs Free-Air Temperature

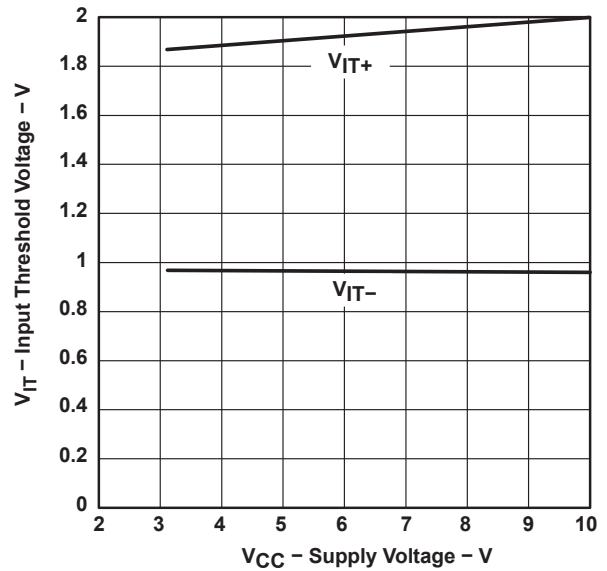
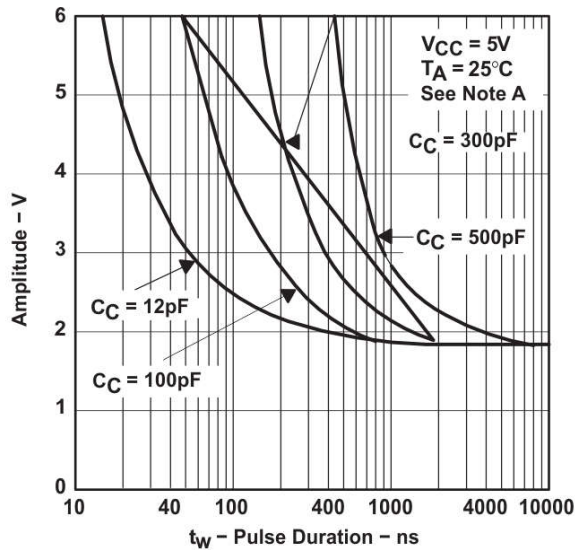


Figure 5-6. Input Threshold Voltage vs Supply Voltage



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0V, does not cause a change of the output level.

Figure 5-7. Noise Rejection

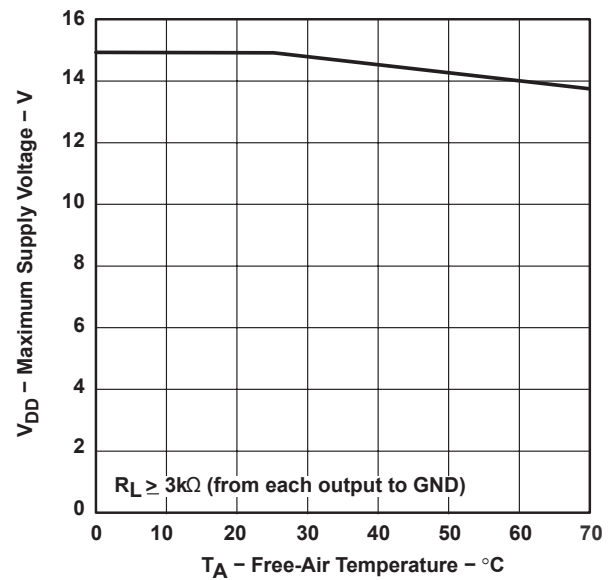


Figure 5-8. Maximum Supply Voltage vs Free-Air Temperature

## 6 Parameter Measurement Information

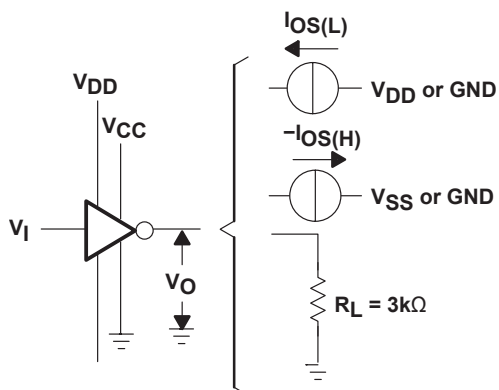


Figure 6-1. Driver Test Circuit for  $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(H)}$ , and  $I_{OS(L)}$

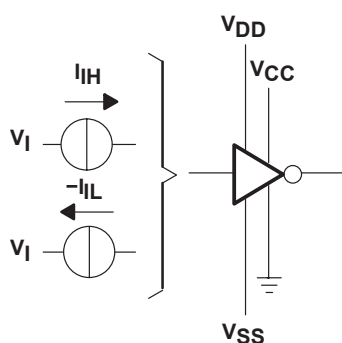
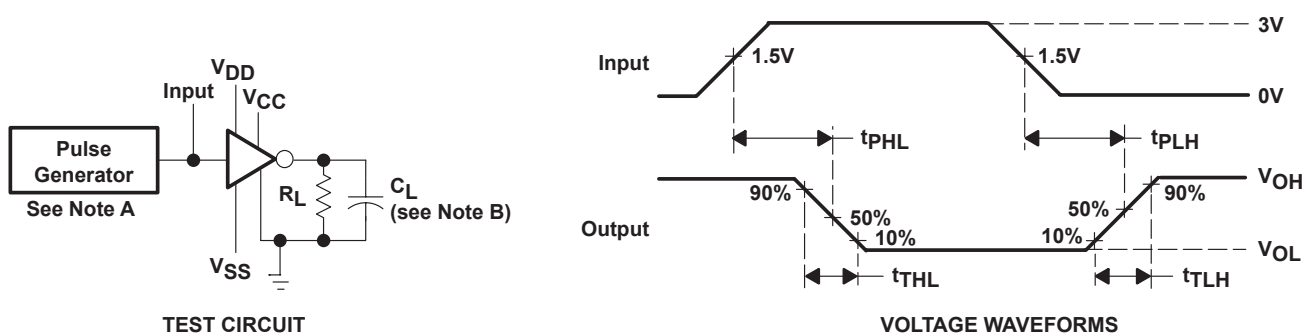


Figure 6-2. Driver Test Circuit for  $I_{IH}$  and  $I_{IL}$



NOTES: A. The pulse generator has the following characteristics:  $t_W = 25\mu s$ ,  $PRR = 20kHz$ ,  $Z_O = 50\Omega$ ,  $t_r = t_f < 50ns$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 6-3. Driver Test Circuit and Voltage Waveforms

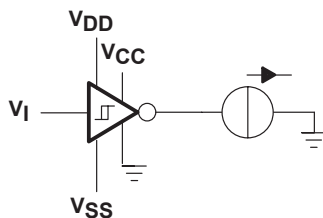


Figure 6-4. Receiver Test Circuit for  $I_{0S}$

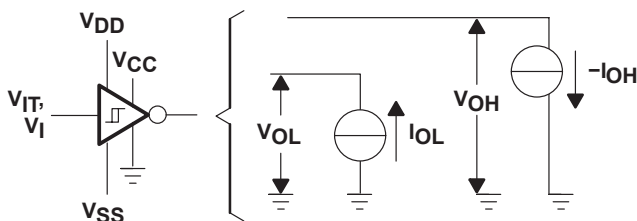
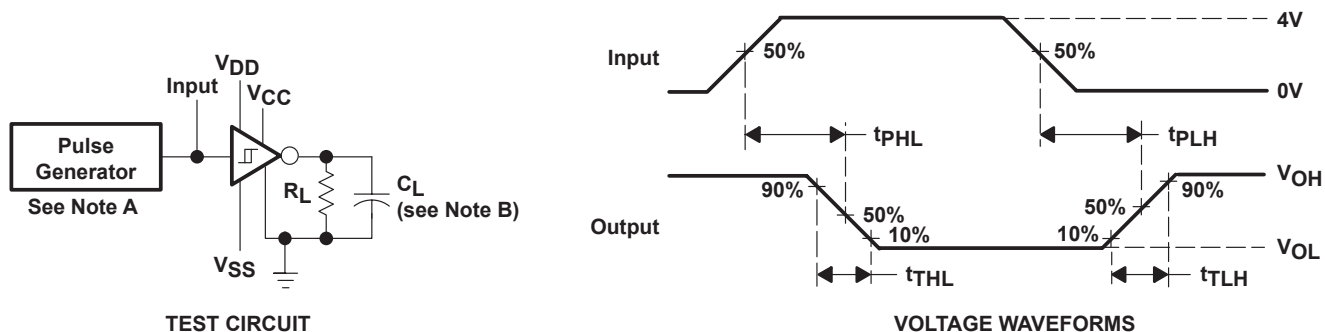


Figure 6-5. Receiver Test Circuit for  $V_{IT}$ ,  $V_{OH}$ , and  $V_{OL}$



NOTES: A. The pulse generator has the following characteristics:  $t_W = 25\mu s$ ,  $PRR = 20kHz$ ,  $Z_O = 50\Omega$ ,  $t_r = t_f < 50ns$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 6-6. Receiver Propagation and Transition Times

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

Diodes placed in series with the VDD and VSS leads protect the GD65232 and GD75232 in the fault condition in which the device outputs are shorted to  $\pm 15\text{V}$  and the power supplies are at low and provide low-impedance paths to ground, see Figure 7-1.

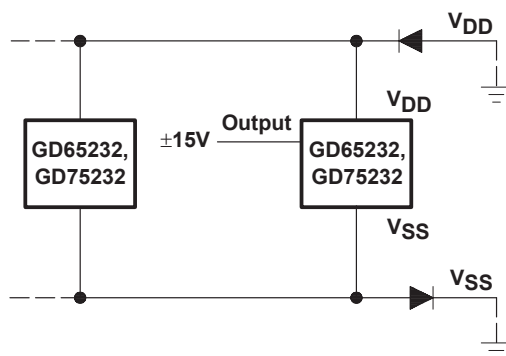


Figure 7-1. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

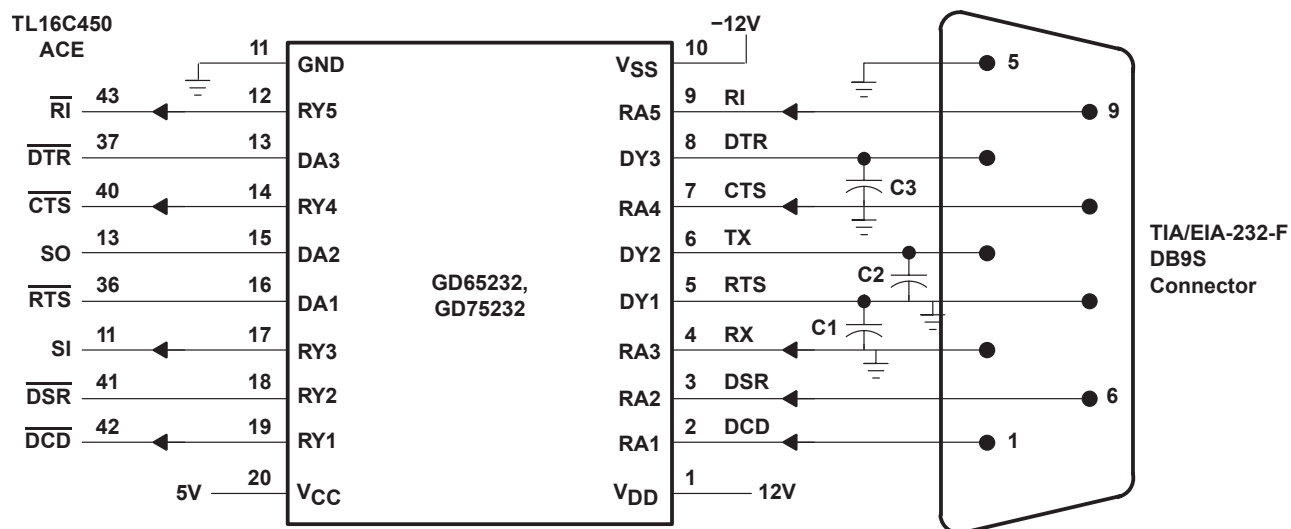
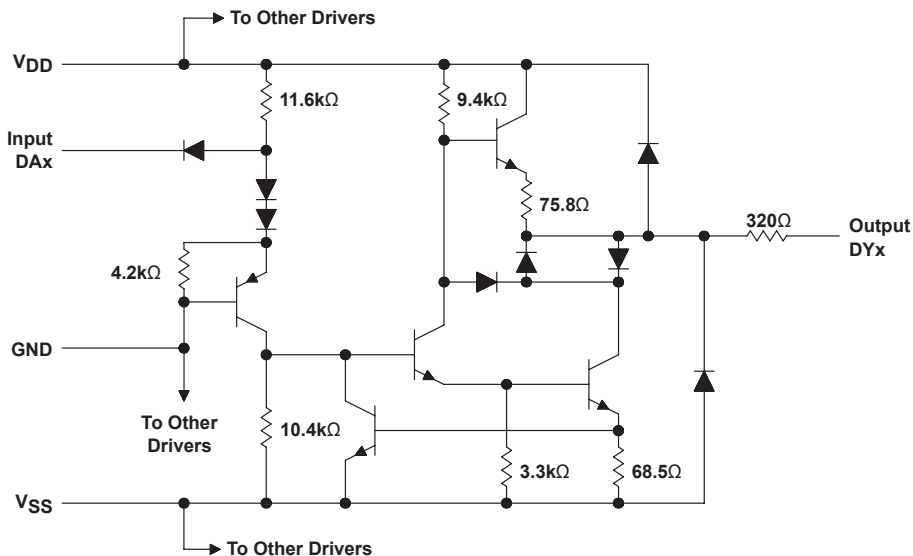


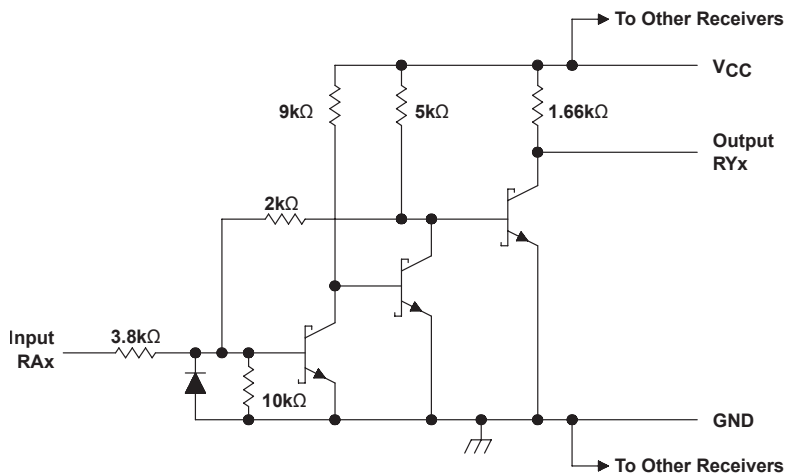
Figure 7-2. Typical Connection

## 7.2 Schematic



Resistor values shown are nominal.

**Figure 7-3. Schematic (each driver)**



**Figure 7-4. Schematic (each receiver)**

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision K (August 2012) to Revision L (August 2024)                                     | Page |
|-------------------------------------------------------------------------------------------------------|------|
| • Changed the numbering format for tables, figures, and cross-references throughout the document..... | 1    |
| • Added the <i>Thermal Information</i> table.....                                                     | 5    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">GD65232DW</a>    | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GD65232             |
| GD65232DW.A                  | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GD65232             |
| <a href="#">GD65232DWR</a>   | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GD65232             |
| GD65232DWR.A                 | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GD65232             |
| <a href="#">GD65232PWR</a>   | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GD65232             |
| GD65232PWR.A                 | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | GD65232             |
| <a href="#">GD75232DBR</a>   | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| GD75232DBR.A                 | Active        | Production           | SSOP (DB)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| <a href="#">GD75232DW</a>    | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| GD75232DW.A                  | Active        | Production           | SOIC (DW)   20  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| <a href="#">GD75232DWR</a>   | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| GD75232DWR.A                 | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| GD75232DWRG4                 | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| <a href="#">GD75232N</a>     | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | GD75232N            |
| GD75232N.A                   | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | GD75232N            |
| <a href="#">GD75232PWR</a>   | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| GD75232PWR.A                 | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | GD75232             |
| <a href="#">GD75232PWRG4</a> | Obsolete      | Production           | TSSOP (PW)   20 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | GD75232             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| GD65232DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| GD65232PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| GD65232PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| GD75232DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| GD75232DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| GD75232DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| GD75232PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| GD75232PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| GD65232DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| GD65232PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| GD65232PWR | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| GD75232DBR | SSOP         | DB              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| GD75232DBR | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| GD75232DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| GD75232PWR | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| GD75232PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| GD65232DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| GD65232DW.A | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| GD75232DW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| GD75232DW   | DW           | SOIC         | 20   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| GD75232DW.A | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| GD75232DW.A | DW           | SOIC         | 20   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| GD75232N    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| GD75232N.A  | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |



## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

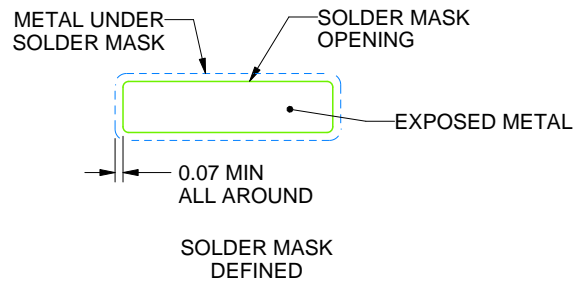
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



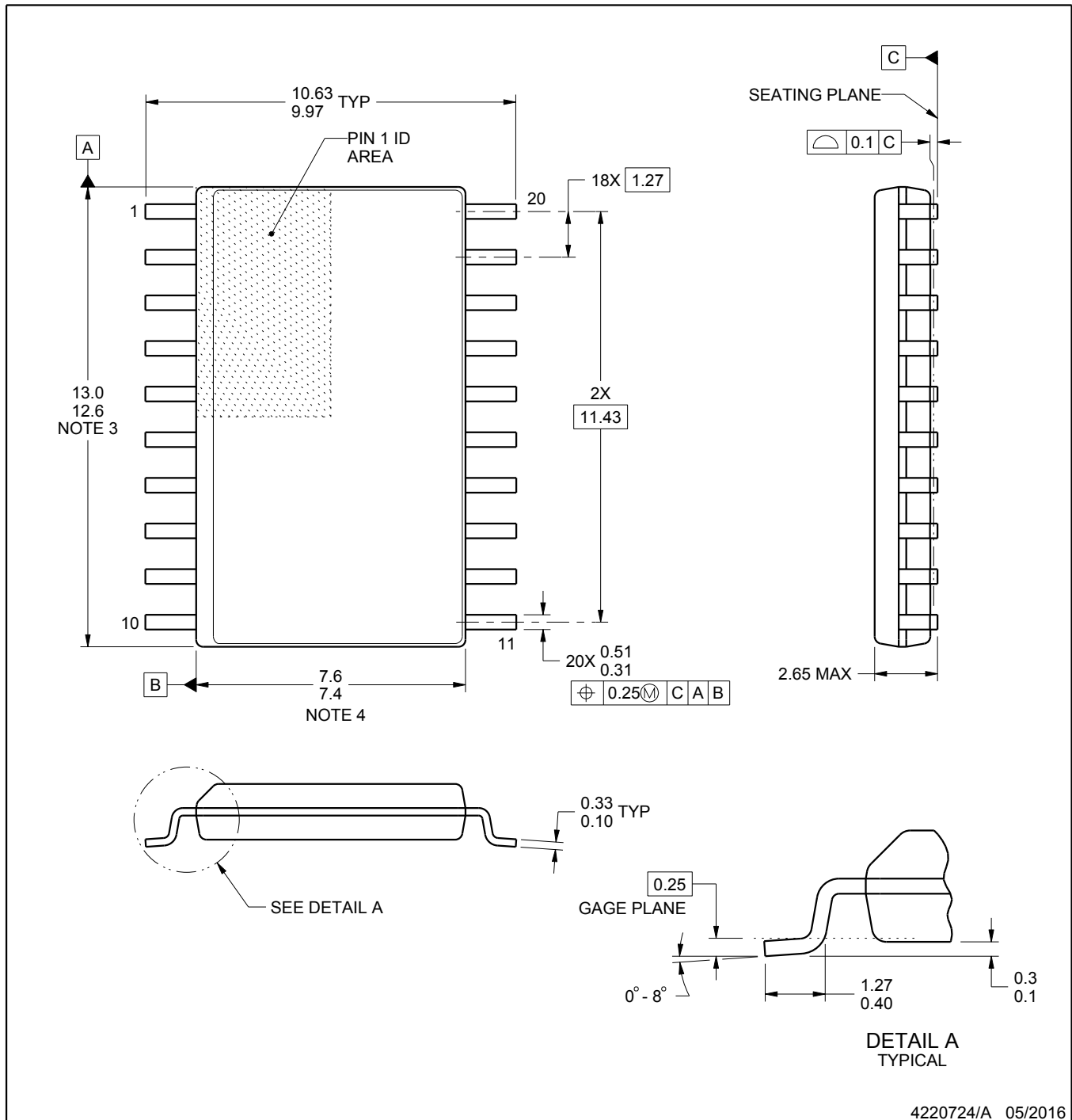
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

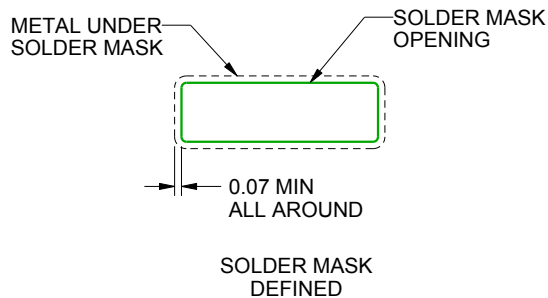
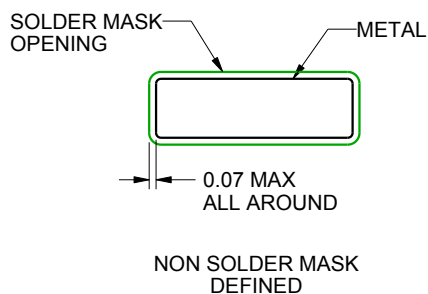
**DW0020A**

## SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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