

3-V to 5.5-V Multichannel RS-232 Line Drivers and Receivers with ± 15 -kV ESD Protection

1 Features

- ESD Protection for RS-232 bus pins
 - ± 15 -kV Human-body model (HBM)
 - ± 8 -kV IEC 61000-4-2, Contact discharge
 - ± 15 -kV IEC 61000-4-2, Air-gap discharge
- Meet or exceed the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operate with 3-V to 5.5-V V_{CC} supply
- Operate up to 1000 kbit/s
- Two drivers and two receivers
- Low standby current . . . 1 μ A Typ
- External capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input with 3.3-V supply

2 Applications

- [Industrial PCs](#)
- [Wired Networking](#)
- [Data center and networking equipment](#)
- [Notebooks](#)
- [Hand-held equipment](#)

3 Description

The SN65C3222E and SN75C3222E consist of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND).

The devices meet the requirements of TIA/EIA-232-F and provide the electrical interface between

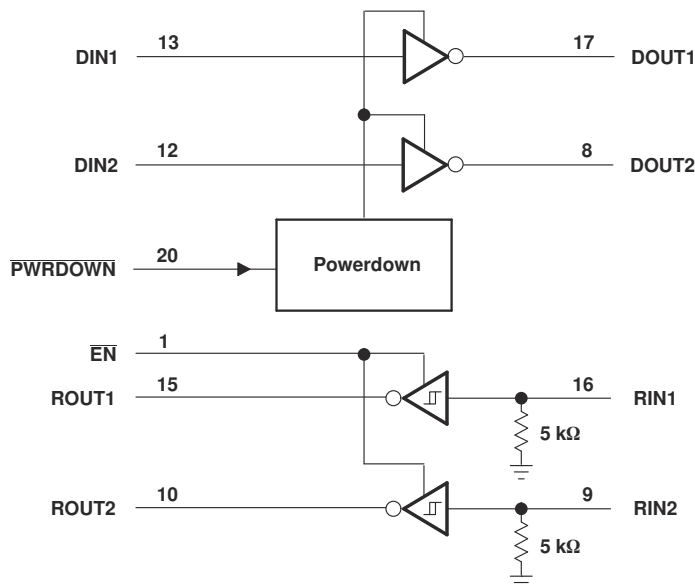
an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at typical data signaling rates up to 1000 kbit/s and are improved drop-in replacements for industry-popular '3222 two-driver, two-receiver functions.

The SN65C3222E and SN75C3222E can be placed in the power-down mode by setting the power-down (PWRDOWN) input low, which draws only 1 μ A from the power supply. When the devices are powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V_+ is lowered to V_{CC} , and V_- is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ($\overline{EN}$) high.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN65C3222E SN75C3222E	DB (SSOP) (20)	10.2 mm x 5.30 mm
	DW (SOIC) (20)	15.4 mm x 7.50 mm
	PW (TSSOP) (20)	7.80 mm v 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers are for the DB, DW, and PW packages.

Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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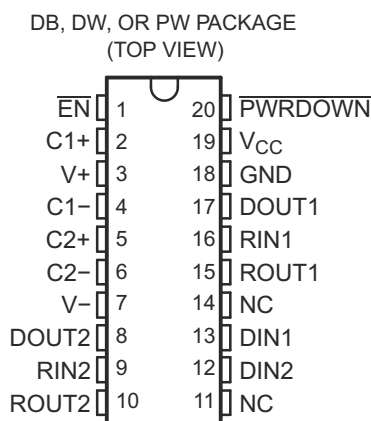
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2006) to Revision B (August 2021)	Page
• Updated the list of <i>Applications</i>	1
• Deleted the <i>Ordering Information</i> table. Removed the RHL package from the <i>Device Information</i> table.....	1
• Added the <i>Device Information</i> table, the <i>Pin Configuration and Functions</i> , the <i>Detailed Description</i> section, the <i>Application and Implementation</i> section.....	1
• Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i>	4
• Added the <i>ESD Ratings</i> table.....	4
• Added the <i>Thermal Information: SN65C3222E</i> table.....	5
• Changed the value of $R_{\theta JA}$ for PW package (previously in the <i>Absolute Maximum Ratings</i> table), and added additional thermal parameters for all packages in the <i>Thermal Information: SN65C3222E</i> table.....	5
• Added separate <i>Thermal Information</i> table for SN75C3222E.....	5

5 Pin Configuration and Functions



NC – No internal connection

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Charge pump capacitor pin
C1-	4	—	Charge pump capacitor pin
C2+	5	—	Charge pump capacitor pin
C2-	6	—	Charge pump capacitor pin
DIN1	13	I	Driver logic input
DIN2	12	I	Driver logic input
DOUT1	17	O	RS-232 driver output
DOUT2	8	O	RS-232 driver output
$\overline{\text{EN}}$	1	I	Receiver enable, active low
GND	18	—	Ground
NC	11,14	—	No internal connection
PWRDOWN	20	I	Driver disable, active low
RIN1	16	I	RS-232 receiver input
RIN2	9	I	RS-232 receiver input
ROUT1	15	O	Receiver logic output
ROUT2	10	O	Receiver logic output
V _{CC}	19	—	Power Supply
V+	3	—	Charge pump capacitor pin
V-	7	—	Charge pump capacitor pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾		−0.3	7	V
V−	Negative-output supply voltage range ⁽²⁾		0.3	−7	V
V+ − V−	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver (EN, PWRDOWN)	−0.3	6	V
		Receiver	−25	25	
V _O	Output voltage range	Driver	−13.2	13.2	V
		Receiver	−0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3,000	V
		RIN1, RIN2, DOUT1 and DOUT2 pins to GND	±15,000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1,500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2, Contact Discharge ⁽¹⁾	±8,000	V
		IEC 61000-4-2, Air Discharge ⁽¹⁾	±15,000	

- (1) For the PW Package of SN65C3222E only, a minimum of 1-μF capacitor is required between V_{CC} and GND to meet the specified IEC 61000-4-2 rating

6.4 Recommended Operating Conditions

See [Figure 9-1](#) and ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage	$V_{CC} = 3.3\text{ V}$		3	3.3	3.6	V
	$V_{CC} = 5\text{ V}$		4.5	5	5.5	
V_{IH} Driver and control high-level input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$	$V_{CC} = 3.3\text{ V}$	2			V
		$V_{CC} = 5\text{ V}$	2.4			
V_{IL} Driver and control low-level input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$				0.8	V
V_I Driver and control input voltage	DIN, $\overline{EN}$, $\overline{PWRDOWN}$		0		5.5	V
V_I Receiver input voltage			-25		25	V
T_A Operating free-air temperature	SN75C3222E		0		70	°C
	SN65C3222E		-40		85	

(1) Test conditions are $C1-C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2-C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Thermal Information: SN65C3222E

THERMAL METRIC ⁽¹⁾		SN65C3222E			UNIT
		DB (SSOP)	DW (SOIC)	PW (TSSOP)	
		20 Pins	20 Pins	20 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	58	94.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (bottom) thermal resistance	33.6	30.0	35.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.4	29.6	45.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	7.7	3.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.9	29.3	45.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.6 Thermal Information: SN75C3222E

THERMAL METRIC ¹		SN75C3222E			UNIT
		DB (SSOP)	DW (SOIC)	PW (TSSOP)	
		20	20	20	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	58	83	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.6	30.0	24.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.4	29.6	39.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	7.7	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.9	29.3	39.0	°C/W

6.7 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current ($\overline{EN}$, $\overline{PWRDOWN}$)			± 0.01	± 1	μA
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND		1	10	μA

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are $C1-C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2-C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.8 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾ (3)	MAX	UNIT
V _{OH} High-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = GND	5	5.4		V
V _{OL} Low-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = V _{CC}	–5	–5.4		V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS} Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V	V _O = 0 V	±35	±60	mA
	V _{CC} = 5.5 V				
r _o Output resistance	V _{CC} , V ₊ , and V _– = 0 V, V _O = ±2 V	300	10M		Ω
I _{OZ} Output leakage current	PWRDOWN = GND	V _{CC} = 3 V to 3.6 V, V _O = ±12 V		±25	μA
		V _{CC} = 4.5 V to 5.5 V, V _O = ±10 V		±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.9 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))

PARAMETER	TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate (See Figure 7-1)	R _L = 3 kΩ, One DOUT switching	C _L = 1000 pF	250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V	1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V	1000		
t _{sk(p)} Pulse skew ⁽²⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 7-2		300		ns
SR(tr) Slew rate, transition region (see Figure 7-1)	R _L = 7 kΩ,	C _L = 150 pF to 1000 pF	8	90	V/μs
		C _L = 1000 pF	12	60	
	R _L = 3 kΩ	C _L = 150 pF to 250 pF	24	150	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.10 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 9-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.3		V
I _{OZ}	Output leakage current	EN = 1		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.11 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

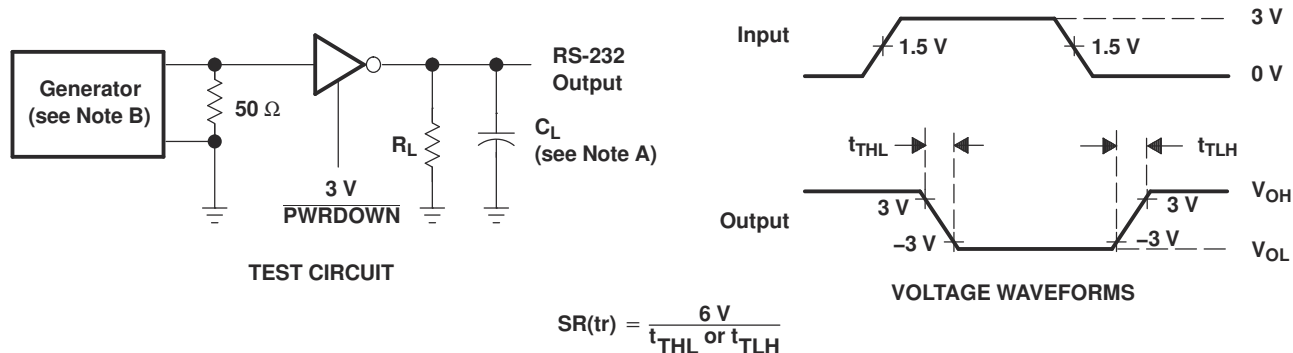
PARAMETER		TEST CONDITIONS ⁽³⁾	TYP ⁽¹⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 7-3	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 7-3	300	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 7-4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 7-4	200	ns
t _{sk(p)}	Pulse skew ⁽²⁾	See Figure 7-3	300	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

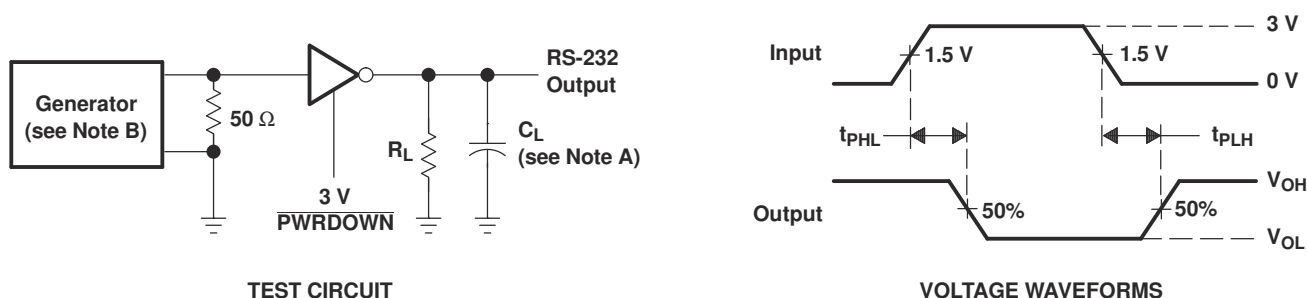
(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

7 Parameter Measurement Information



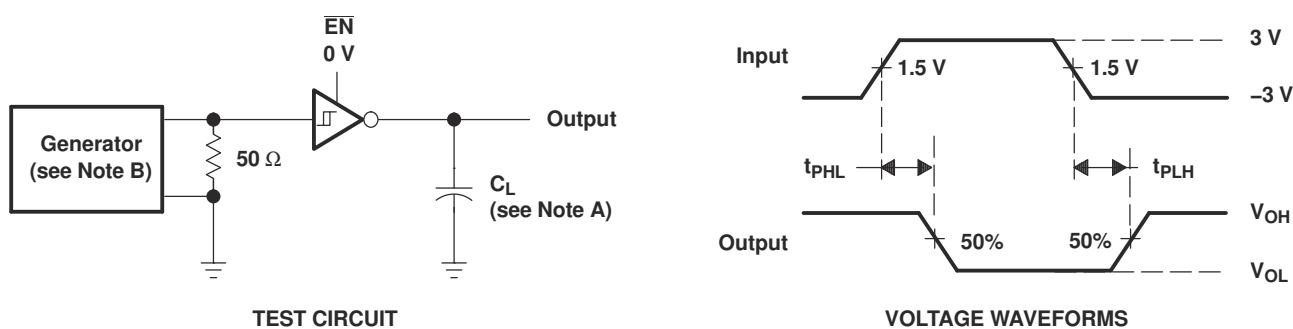
- A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7-1. Driver Slew Rate



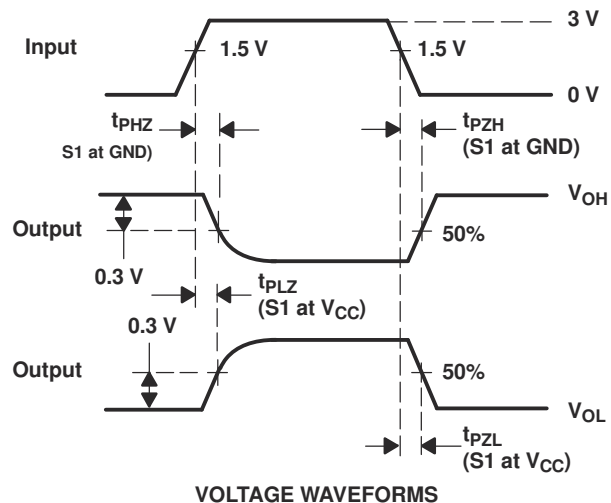
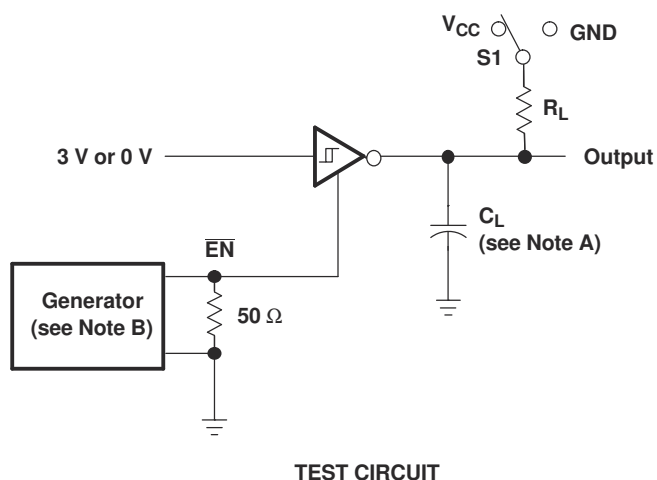
- A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7-2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7-3. Receiver Propagation Delay Times

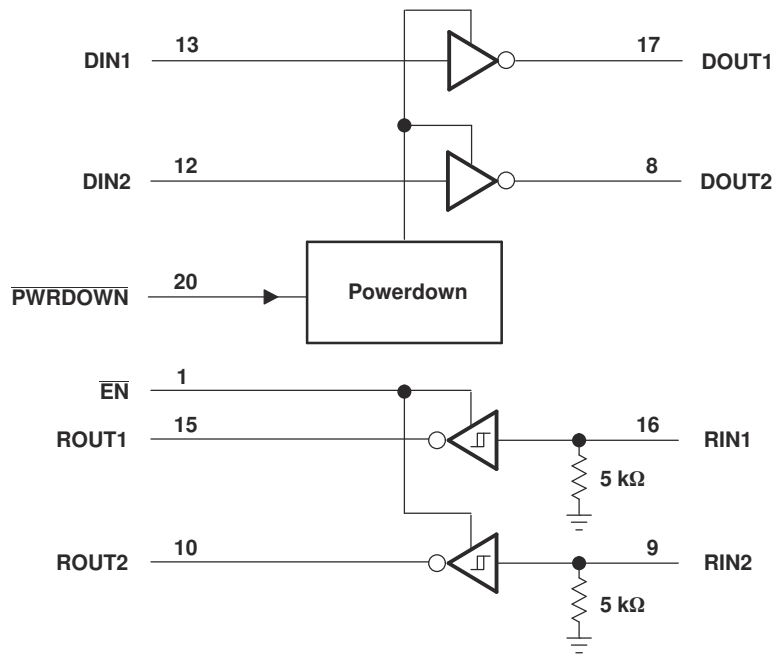


- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 7-4. Receiver Enable and Disable Times

8 Detailed Description

8.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

Figure 8-1. Logic Diagram (Positive Logic)

8.2 Device Functional Modes

Table 8-1. Function Tables: Each Driver

INPUTS ⁽¹⁾		OUTPUT DOUT
DIN	PWRDOWN	
X	L	Z
L	H	H
H	H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 8-2. Function Table: Each Receiver

INPUTS ⁽¹⁾		OUTPUT ROUT
RIN	EN	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

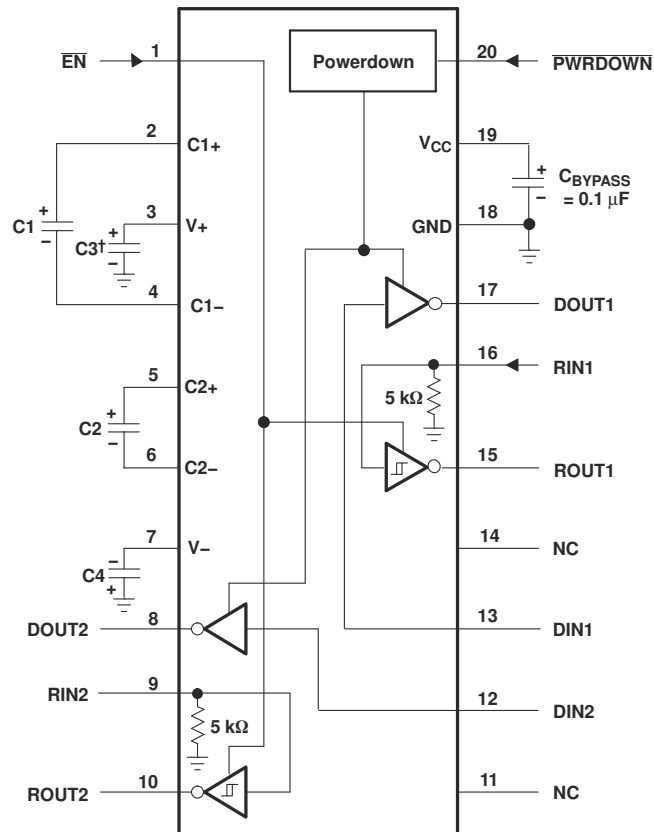
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 9-1. Typical Operating Circuit and Capacitor Values

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3222EDB	Active	Production	SSOP (DB) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU222E
SN65C3222EDB.A	Active	Production	SSOP (DB) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU222E
SN65C3222EDBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU222E
SN65C3222EDBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU222E
SN65C3222EDW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3222E
SN65C3222EDW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3222E
SN65C3222EDWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3222E
SN65C3222EDWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3222E
SN65C3222EPWR	NRND	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU222E
SN65C3222EPWR.A	NRND	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MU222E
SN75C3222EPW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	0 to 70	MY222E

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

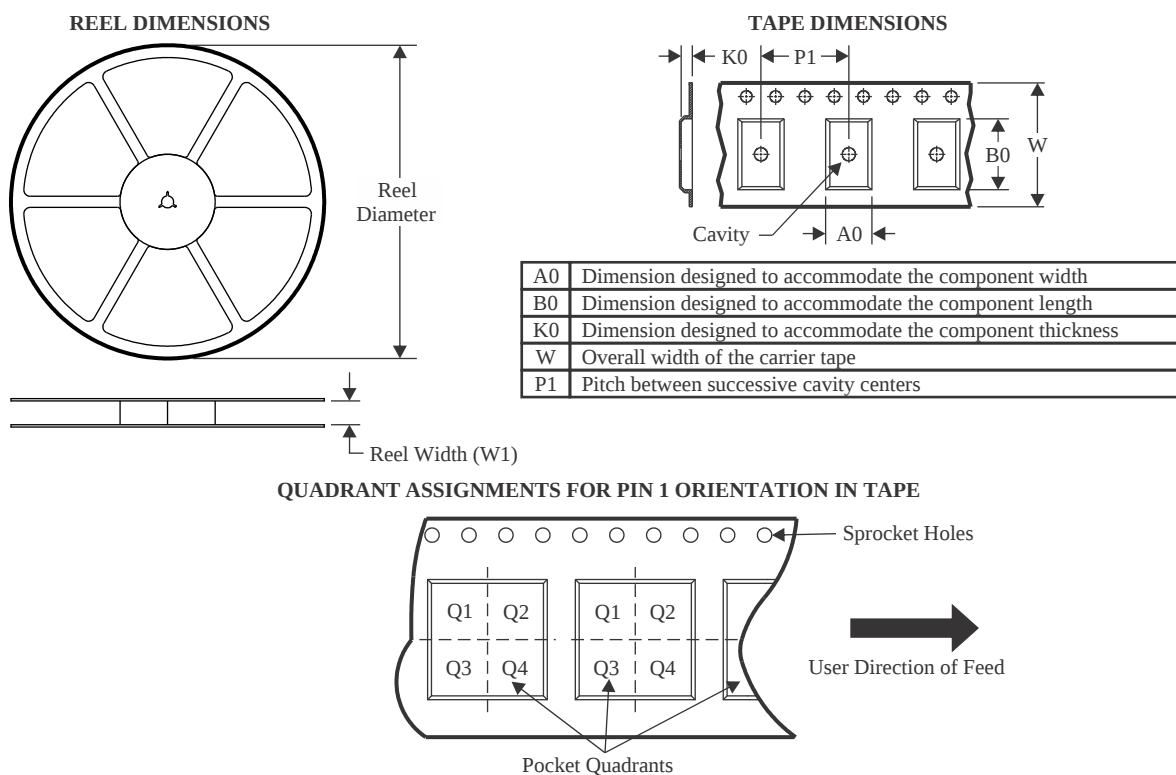
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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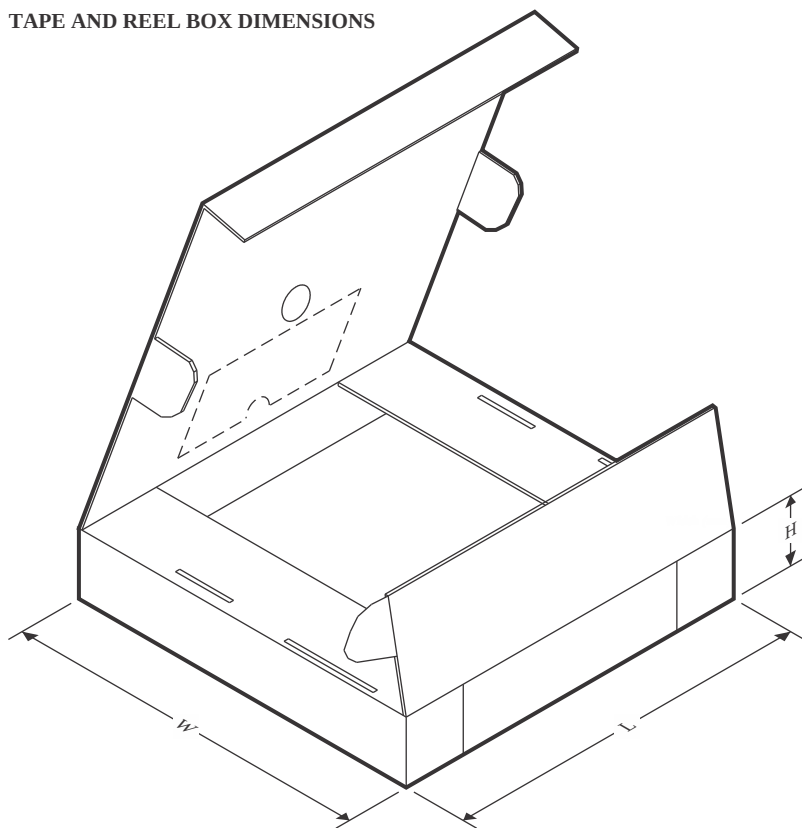
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3222EDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN65C3222EDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN65C3222EPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3222EDBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN65C3222EDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN65C3222EPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

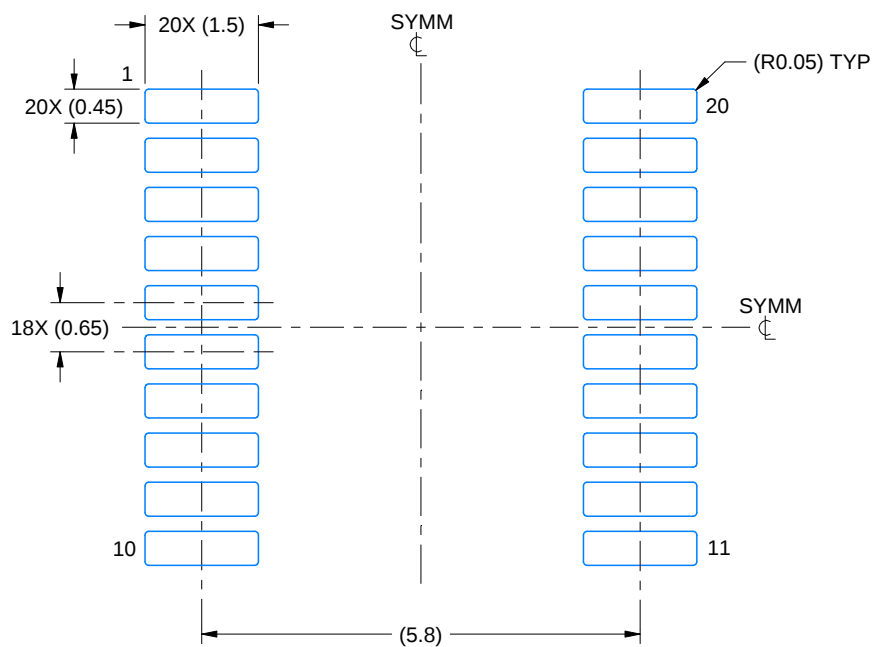
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3222EDB	DB	SSOP	20	70	530	10.5	4000	4.1
SN65C3222EDB.A	DB	SSOP	20	70	530	10.5	4000	4.1
SN65C3222EDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65C3222EDW.A	DW	SOIC	20	25	507	12.83	5080	6.6

EXAMPLE BOARD LAYOUT

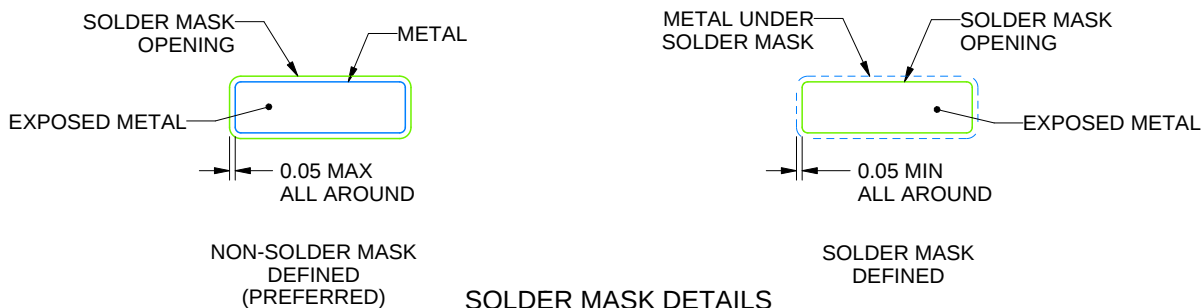
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

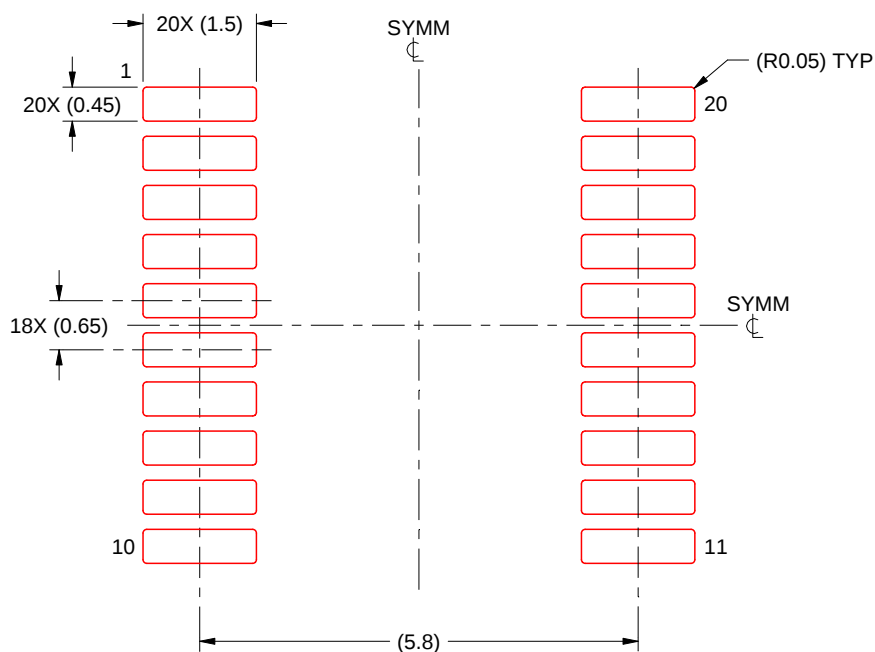
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

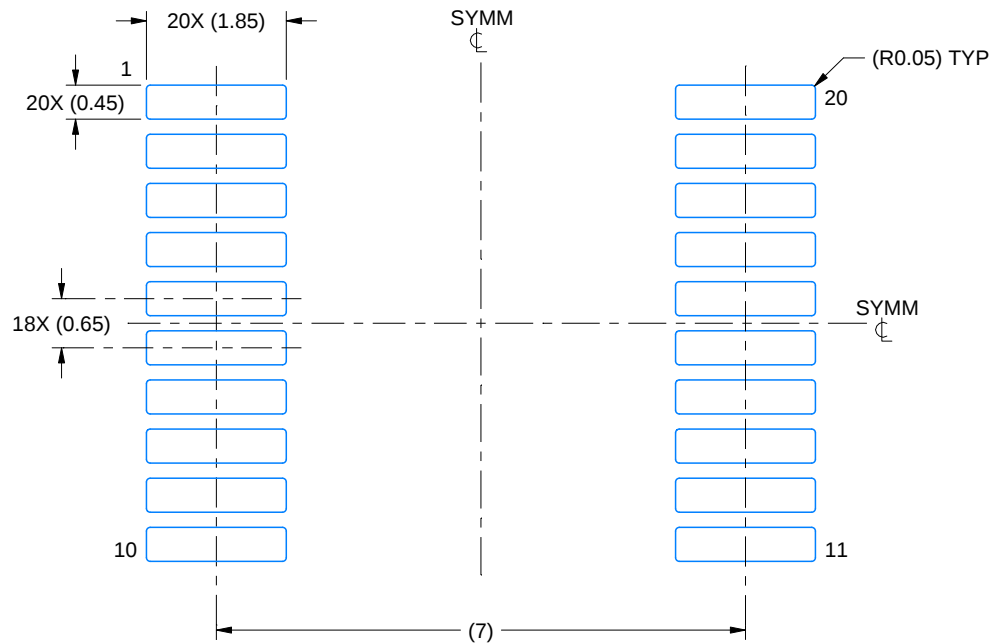
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

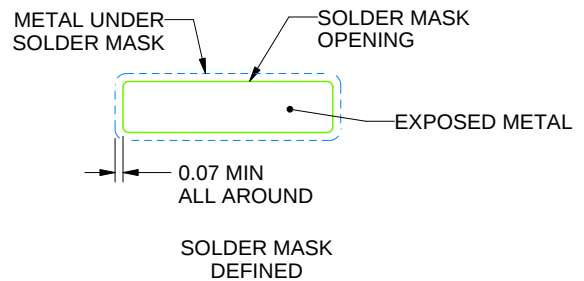
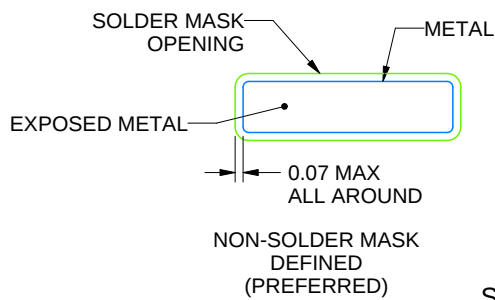
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

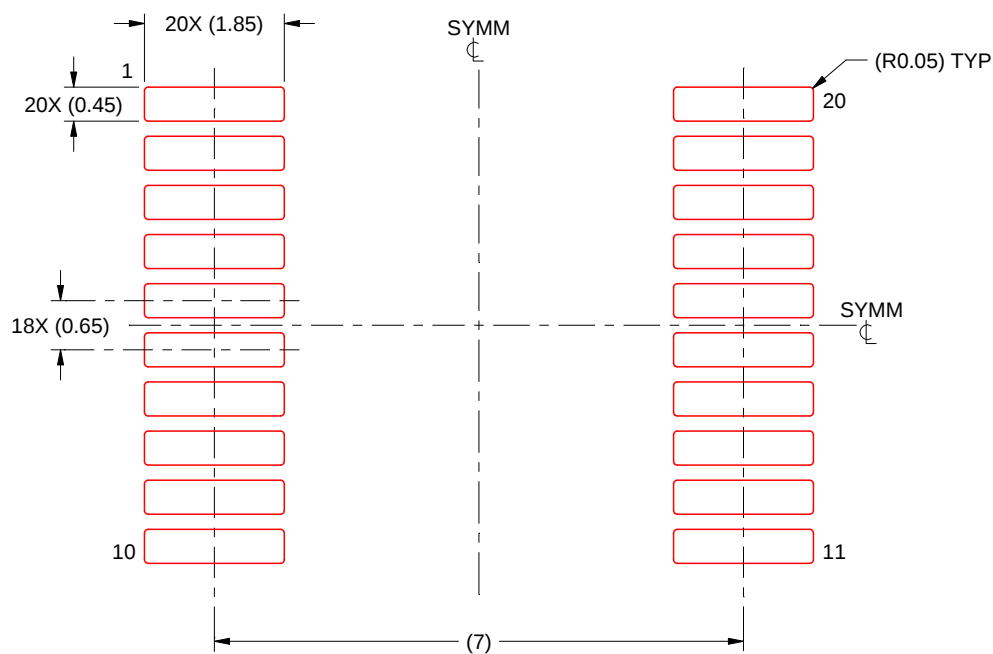
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

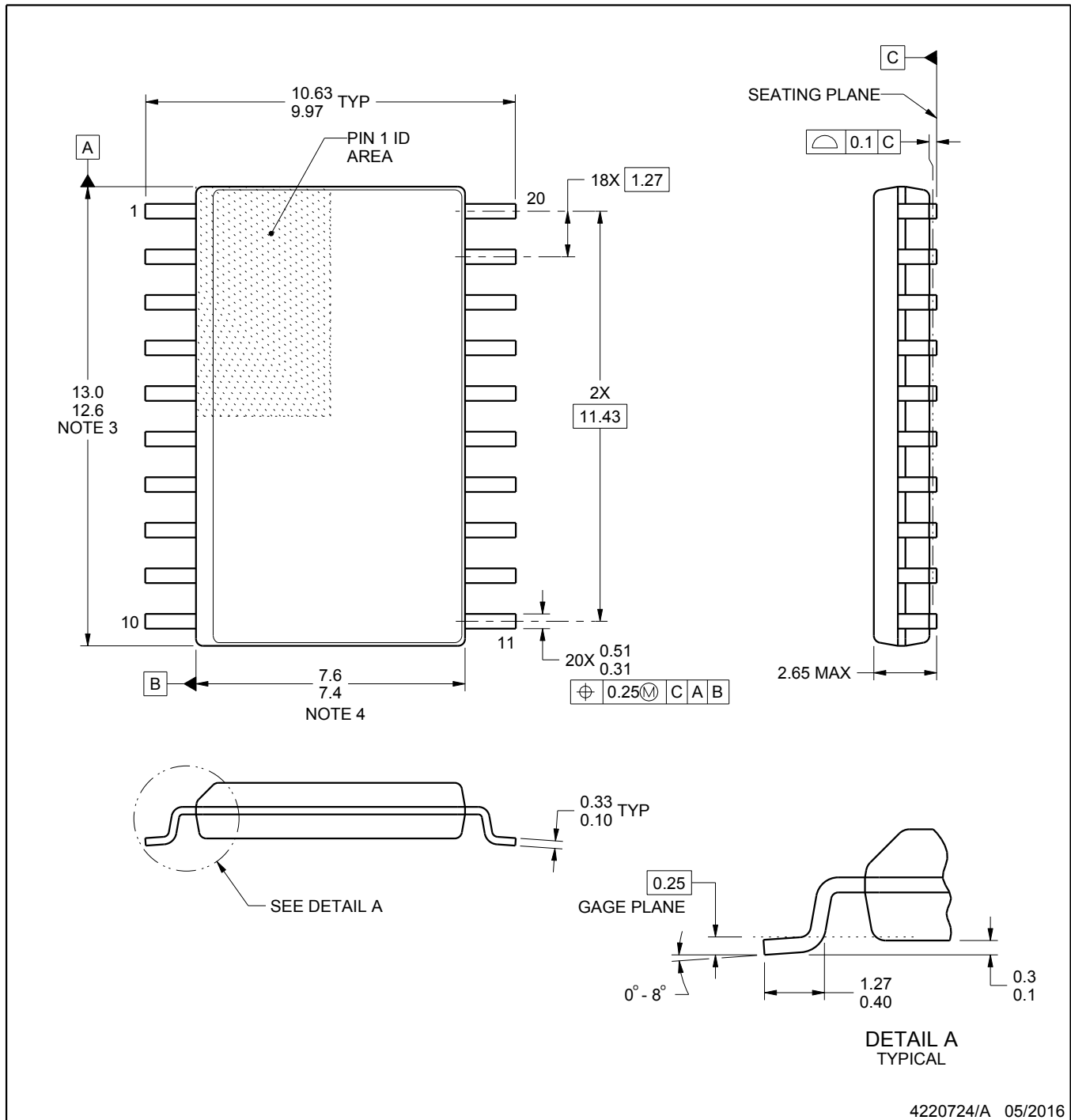
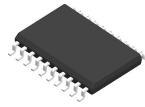


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220724/A 05/2016

NOTES:

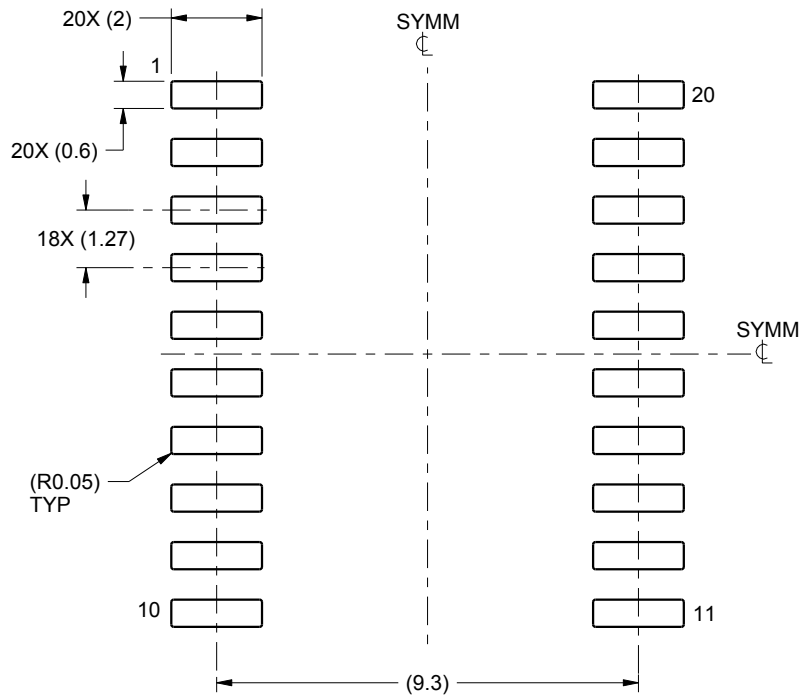
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

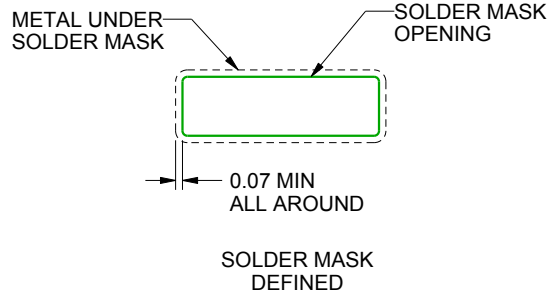
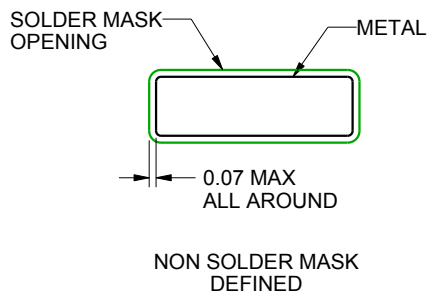
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

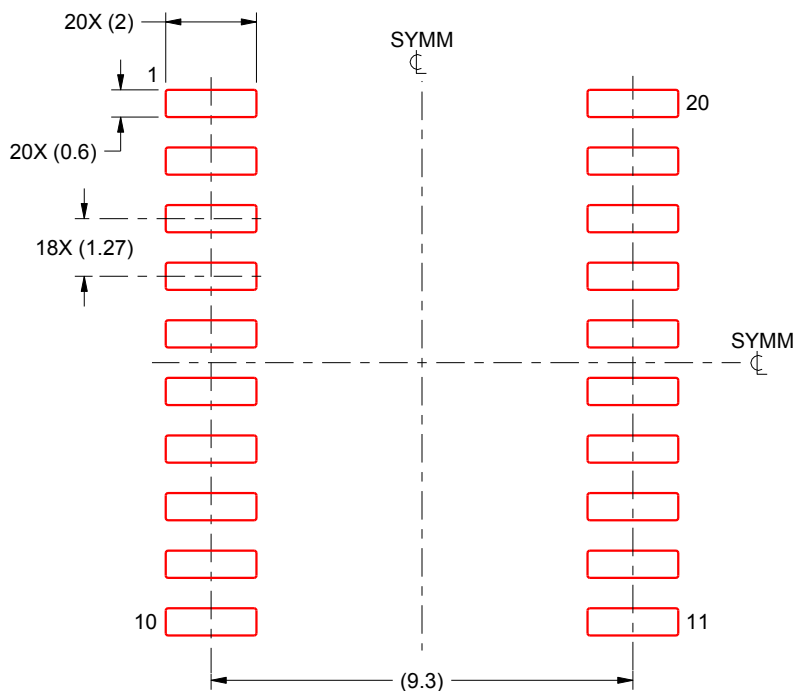
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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