HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

FEATURES

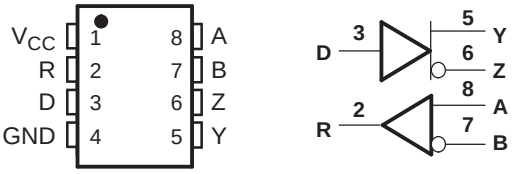
- **Low-Voltage Differential 50-Ω Line Drivers and Receivers**
- **Typical Full-Duplex Signaling Rates of 100 Mbps (See Table 1)**
- **Bus-Terminal ESD Exceeds 12 kV**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 340 mV With a 50-Ω Load**
- **Valid Output With as Little as 50-mV Input Voltage Difference**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typical**
  - **Receiver: 3.7 ns Typical**
- **Power Dissipation at 200 MHz**
  - **Driver: 50 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Input Levels Are 5-V Tolerant**
- **Driver Is High Impedance When Disabled or With V_{CC} < 1.5 V**
- **Receiver Has Open-Circuit Failsafe**

DESCRIPTION

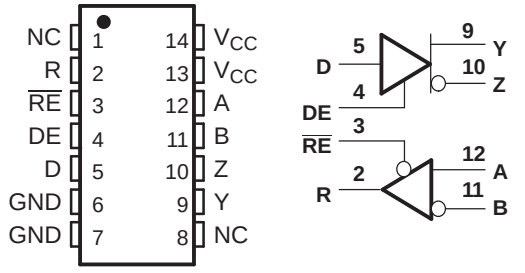
The SN65LVDM179, SN65LVDM180, SN65LVDM050, and SN65LVDM051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve high signaling rates. These circuits are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts, except that the output current of the drivers is doubled. This modification provides a minimum differential output voltage magnitude of 247 mV across a 50-Ω load simulating two transmission lines in parallel. This allows having data buses with more than one driver or with two line termination resistors. The receivers detect a voltage difference of 50 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of these devices and signaling techniques is point-to-point half duplex, baseband data transmission over a controlled impedance media of approximately 100 Ω characteristic impedance.

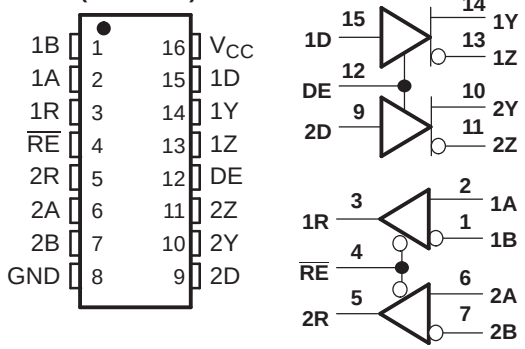
SN65LVDM179D (Marked as **DM179** or **LVM179**)
SN65LVDM179DGK (Marked as **M79**)
(TOP VIEW)



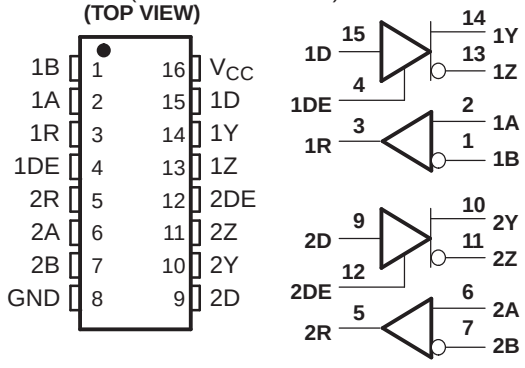
SN65LVDM180D (Marked as **LVDM180**)
SN65LVDM180PW (Marked as **LVDM180**)
(TOP VIEW)



SN65LVDM050D (Marked as **LVDM050**)
SN65LVDM050PW (Marked as **LVDM050**)
(TOP VIEW)



SN65LVDM051D (Marked as **LVDM051**)
SN65LVDM051PW (Marked as **LVDM051**)
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application-specific characteristics.

The SN65LVDM179, SN65LVDM180, SN65LVDM050, and SN65LVDM051 are characterized for operation from –40°C to 85°C.

Table 1. Maximum Recommended Operating Speeds

Part Number	All Buffers Active	Rx Buffer Only	Tx Buffer Only
SN65LVDM179	150 Mbps	150 Mbps	500 Mbps
SN65LVDM180	150 Mbps	150 Mbps	500 Mbps
SN65LVDM050	100 Mbps	100 Mbps	400 Mbps
SN65LVDM051	100 Mbps	100 Mbps	400 Mbps

AVAILABLE OPTIONS

T_A	PACKAGE		
	SMALL OUTLINE (D)	SMALL OUTLINE (DGK)	SMALL OUTLINE (PW)
–40°C to 85°C	SN65LVDM050D	—	SN65LVDM050PW
	SN65LVDM051D	—	SN65LVDM051PW
	SN65LVDM179D	SN65LVDM179DGK	—
	SN65LVDM180D	—	SN65LVDM180PW

FUNCTION TABLES

SN65LVDM179 RECEIVER

INPUTS	OUTPUT(1)
$V_{ID} = V_A – V_B$	R
$V_{ID} \geq 50$ mV	H
50 MV < V_{ID} < 50 mV	?
$V_{ID} \leq –50$ mV	L
Open	H

(1) H = high level, L = low level, ? = indeterminate

SN65LVDM179 DRIVER

INPUT(1)	OUTPUTS(1)	
D	Y	Z
L	L	H
H	H	L
Open	L	H

(1) H = high level, L = low level

SN65LVDM180, SN65LVDM050, and SN65LVDM051 RECEIVER

INPUTS(1)		OUTPUT(1)
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
50 MV < V_{ID} < 50 mV	L	?
$V_{ID} \leq -50$ mV	L	L
Open	L	H
X	H	Z

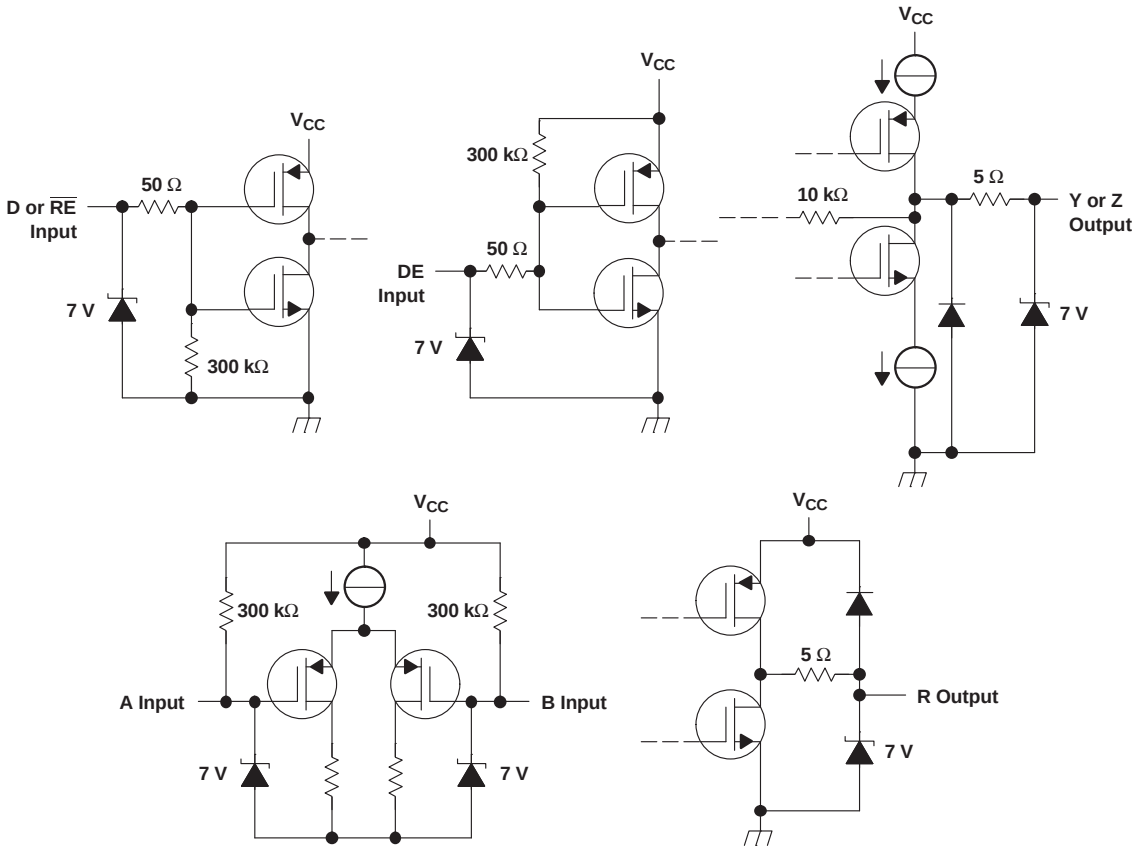
(1) H = high level, L = low level, Z = high impedance, X = don't care

SN65LVDM180, SN65LVDM050, and SN65LVDM051 DRIVER

INPUTS(1)		OUTPUTS(1)	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, Z = high impedance, X = don't care

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage range(2)		–0.5 V to 4 V
	Voltage range	D, R, DE, $\overline{RE}$	–0.5 V to 6 V
		Y, Z, A, and B	–0.5 V to 4 V
	Electrostatic discharge	Y, Z, A, B , and GND(3)	CLass 3, A:12 kV, B:600 V
		All	Class 3, A:7 kV, B:500 V
	Continuous power dissipation		See Dissipation Rating Table
	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 85°C$ POWER RATING
D(8)	635 mW	5.1 mW/°C	330 mW
D(14)	987 mW	7.9 mW/°C	513 mW
D(16)	1110 mW	8.9 mW/°C	577 mW
DGK	424 mW	3.4 mW/°C	220 mW
PW (14)	736 mW	5.9 mW/°C	383 mW
PW (16)	839 mW	6.7 mW/°C	437 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_O	Driver output voltage	0		2.4	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
$\lvert V_{ID} \rvert$	Magnitude of differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 6)	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
		V_{CC}-0.8			
T_A	Operating free-air temperature	—40		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	SN65LVDM179	No receiver load, driver R_L = 50 Ω		10	15	mA
		SN65LVDM180	Driver and receiver enabled, no receiver load, driver R_L = 50 Ω		10	15	mA
			Driver enabled, receiver disabled, R_L = 50 Ω		9	13	
			Driver disabled, receiver enabled, no load		1.7	5	
			Disabled		0.5	2	
		SN65LVDM050	Drivers and receivers enabled, no receiver loads, driver R_L = 50 Ω		19	27	mA
			Drivers enabled, receivers disabled, R_L = 50 Ω		16	24	
			Drivers disabled, receivers enabled, no loads		4	6	
			Disabled		0.5	1	
		SN65LVDM051	Drivers enabled, no receiver loads, driver R_L = 50 Ω		19	27	mA
			Drivers disabled, no loads		4	6	

(1) All typical values are at 25°C and with a 3.3 V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude		R_L = 50 Ω, See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50(1)		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current	DE	V_{IH} = 5 V	–20	–0.5		µA
		D			2	20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8 V	–10	–0.5		µA
		D			2	10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0 V		7	10	mA
			V_{OD} = 0 V		7	10	
I_{OZ}	High-impedance output current		V_O = 0 V or 2.4 V, other output at 1.2 V, DE AT 0.8 V	–47		47	µA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0 V, V_O = 0 V or 2.4 V, other output at 1.2 V, DE AT 0.8 V	–47		47	µA
C_{IN}	Input capacitance				3		pF

(1) The algebraic convention in which the least positive (most negative) value is designated minimum is used in this datasheet.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 5 and Table 2			50	mV
V_{IT-}	Negative-going differential input voltage threshold		–50			
V_{OH}	High-level output voltage	I_{OH} = -8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)	V_I = 0	–20	–11		µA
		V_I = 2.4 V		–3	–1.2	
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0	–20		20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current	V_O = 0 or 5 V	–10		10	µA
C_I	Input capacitance			5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50Ω, C_L = 10 pF, See Figure 6		1.7	2.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.7	2.7	ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.6	1	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)			250		ps
$t_{sk(o)}$	Channel-to-channel output skew(2)			100		ps
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 7		6	10	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			6	10	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			4	10	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5	10	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 6		3.7	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.7	4.5	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)			0.1		ns
$t_{sk(o)}$	Channel-to-channel output skew			0.2		ns
$t_{sk(pp)}$	Part-to-part skew(2)				1	ns
t_r	Output signal rise time	C_L = 10 pF, See Figure 6		0.7	1.5	ns
t_f	Output signal fall time			0.9	1.5	ns
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 7		2.5		ns
t_{PZL}	Propagation delay time, low-level-to-low-impedance output			2.5		ns
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output			7		ns
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output			4		ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

DRIVER

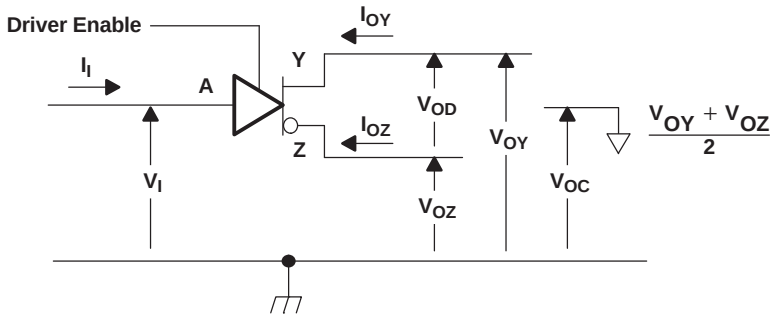
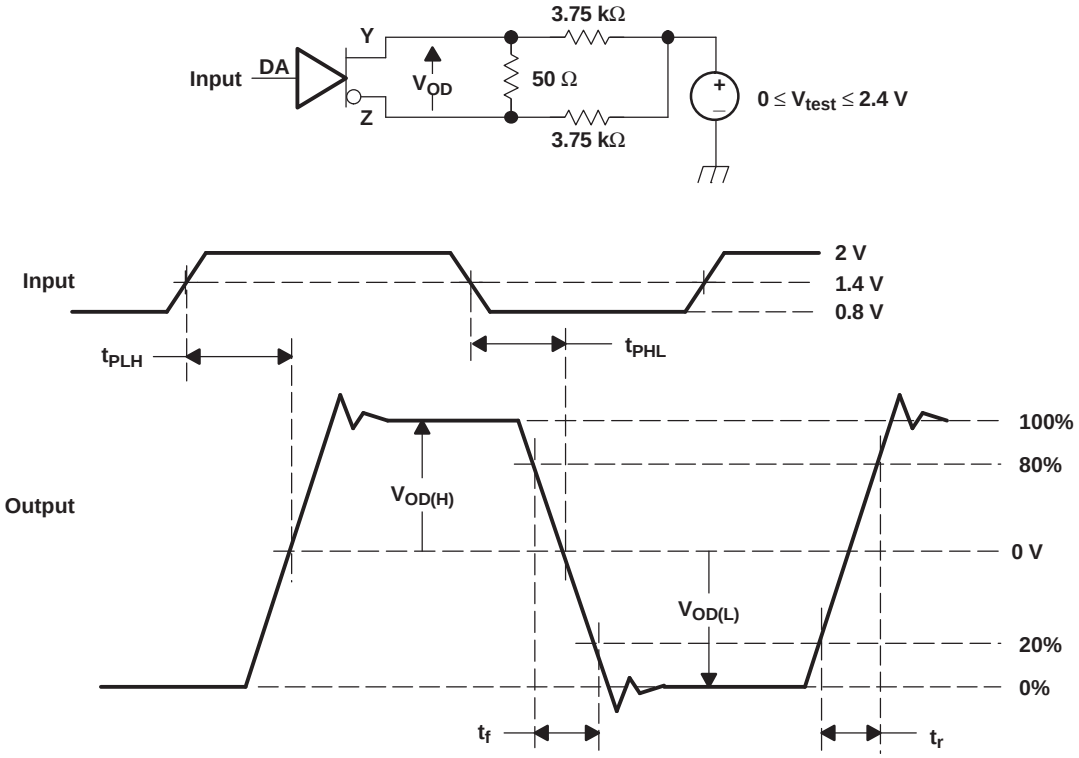


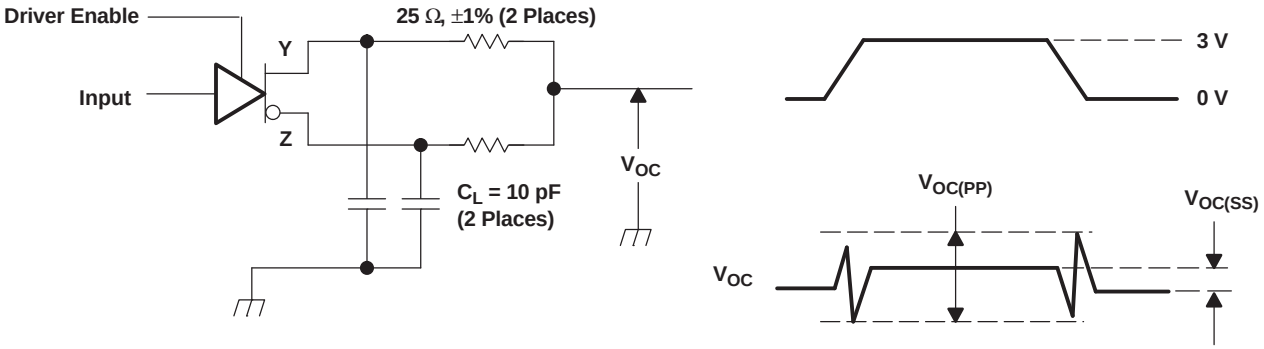
Figure 1. Driver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

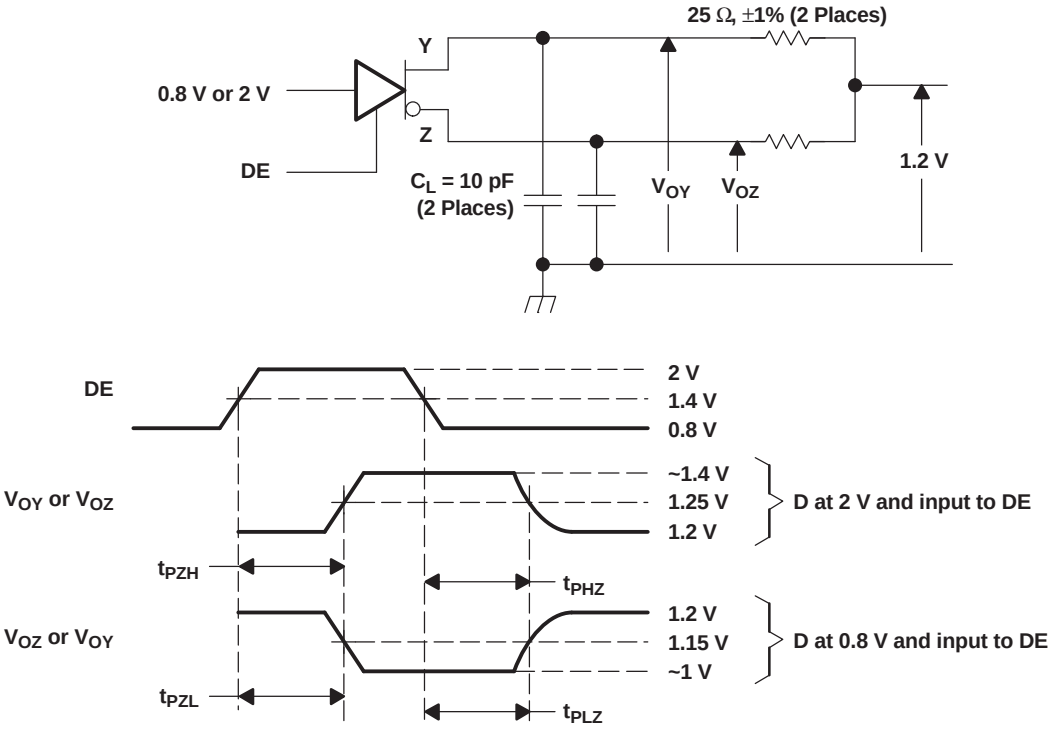
Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

RECEIVER

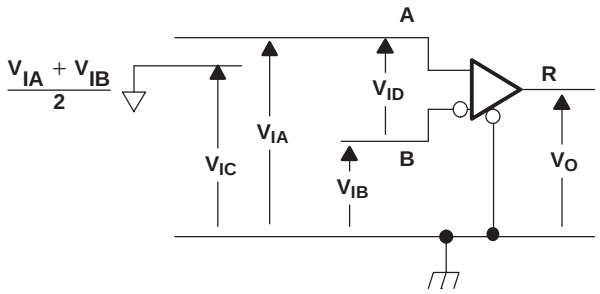
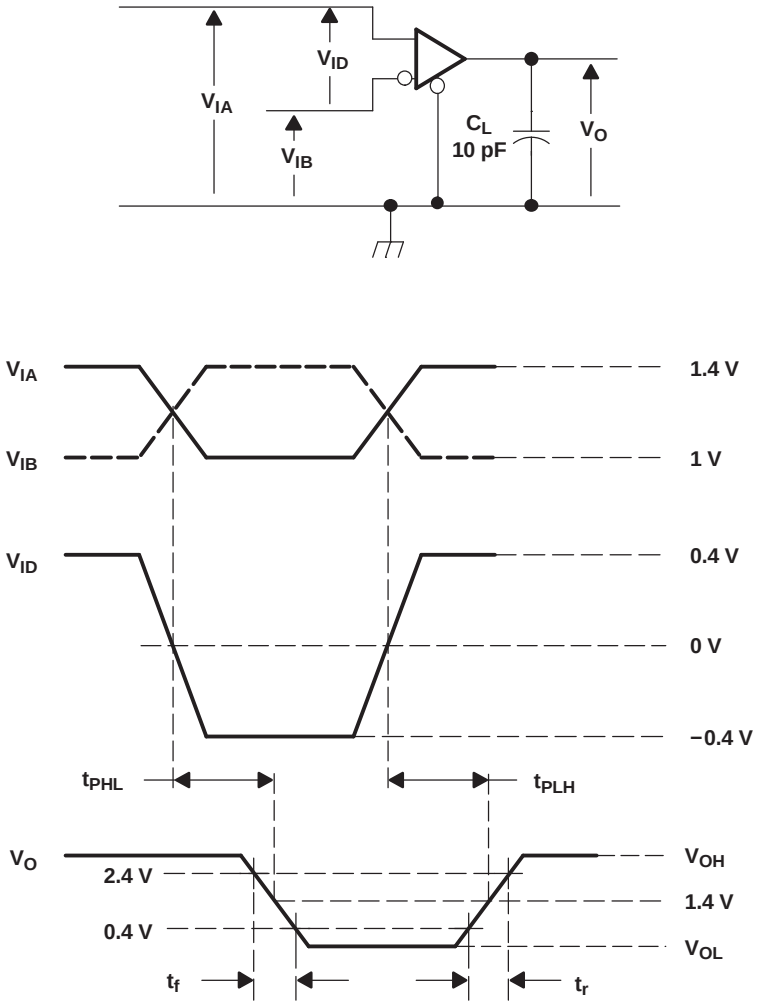


Figure 5. Receiver Voltage Definitions

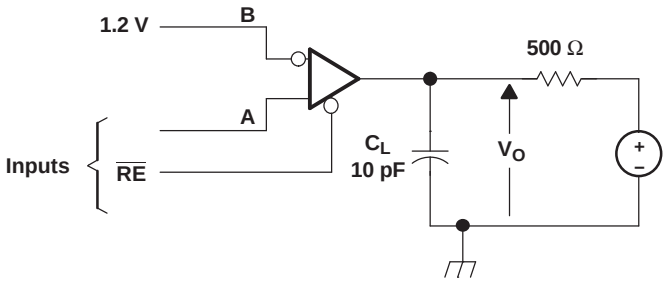
Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.225	1.175	50	1.2
1.175	1.225	–50	1.2
2.375	2.325	50	2.35
2.325	2.375	–50	2.35
0.05	0	50	0.05
0	0.05	–50	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

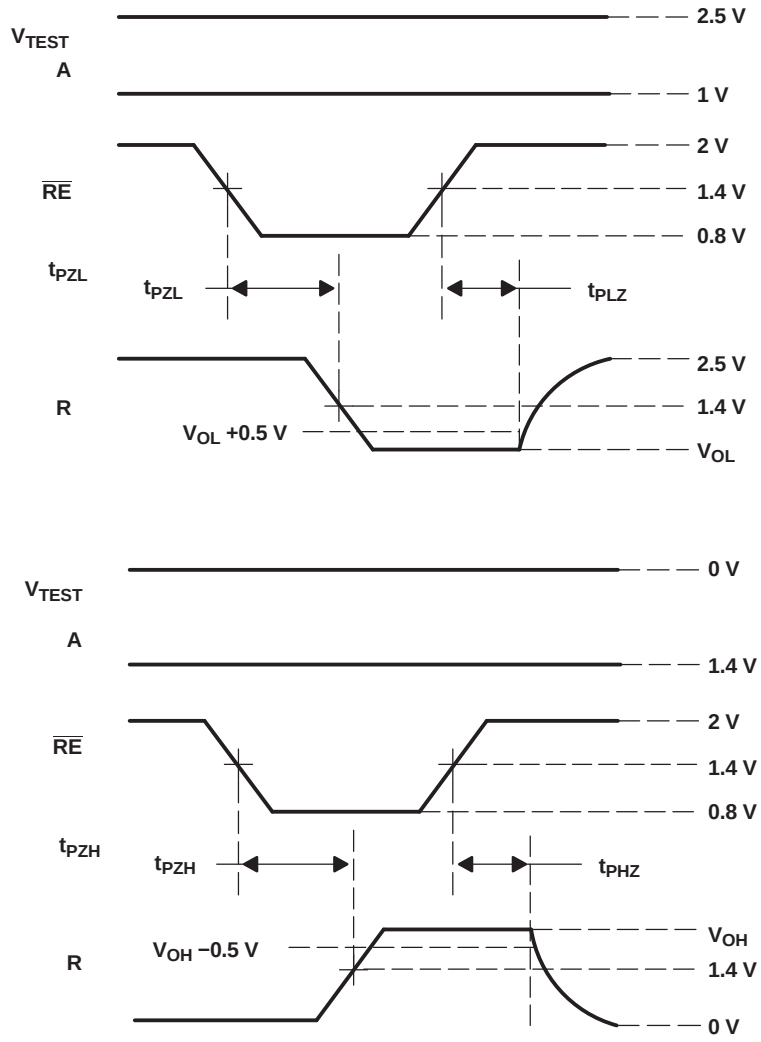


Figure 7. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

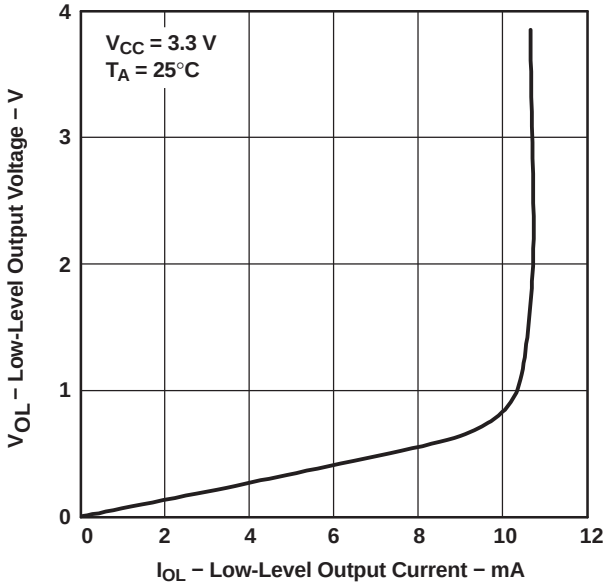


Figure 8.

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

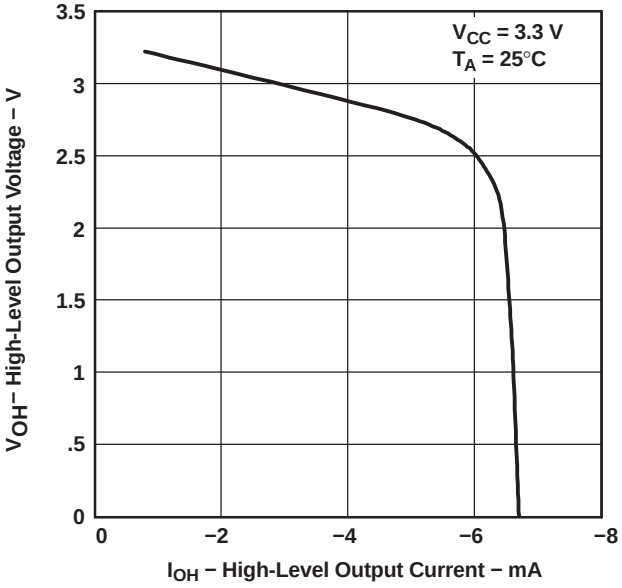


Figure 9.

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

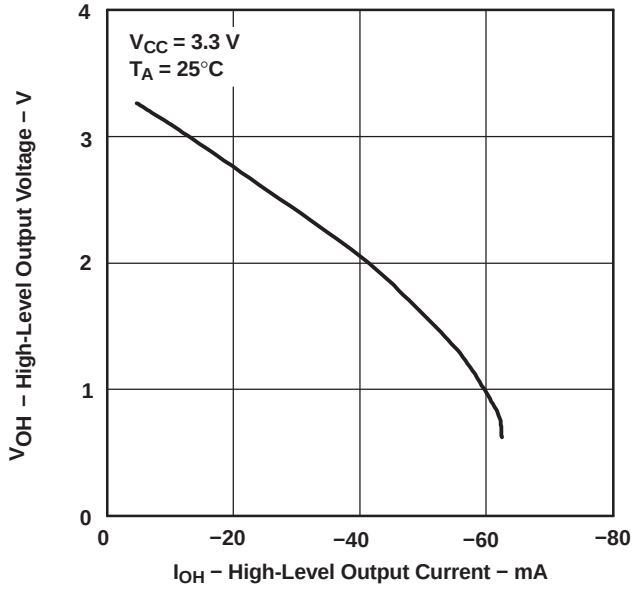


Figure 10.

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

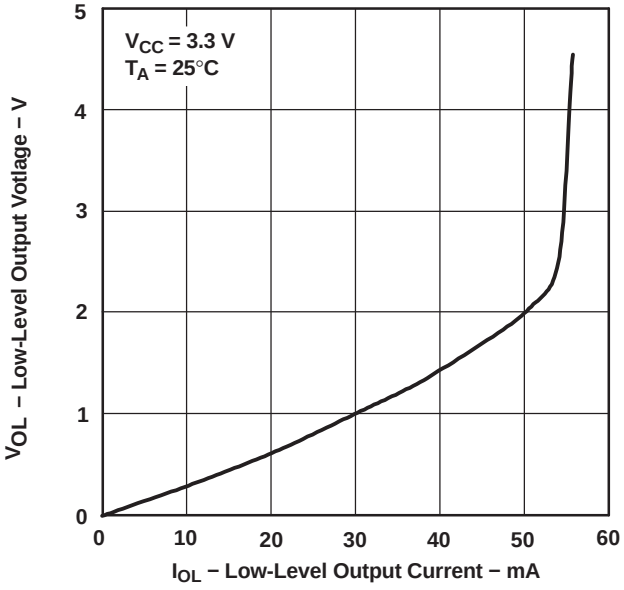


Figure 11.

TYPICAL CHARACTERISTICS (continued)

DRIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

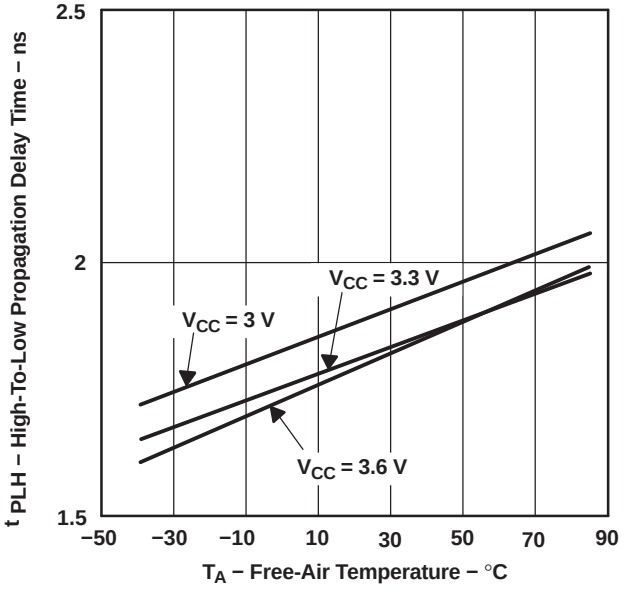


Figure 12.

DRIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

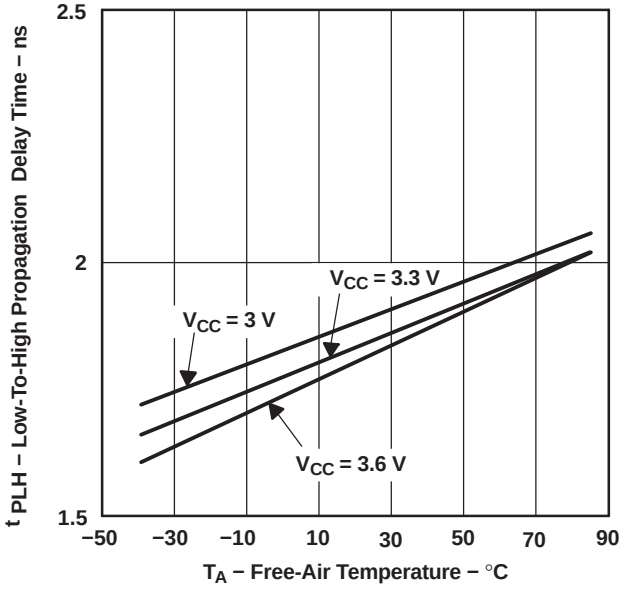


Figure 13.

RECEIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

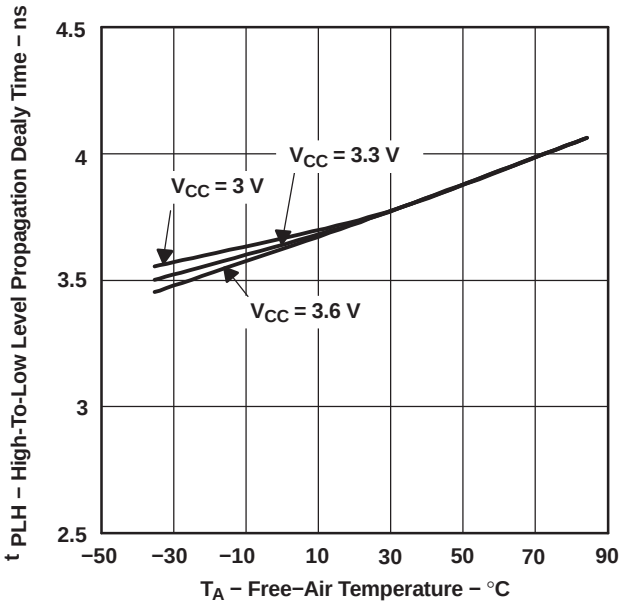


Figure 14.

RECEIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

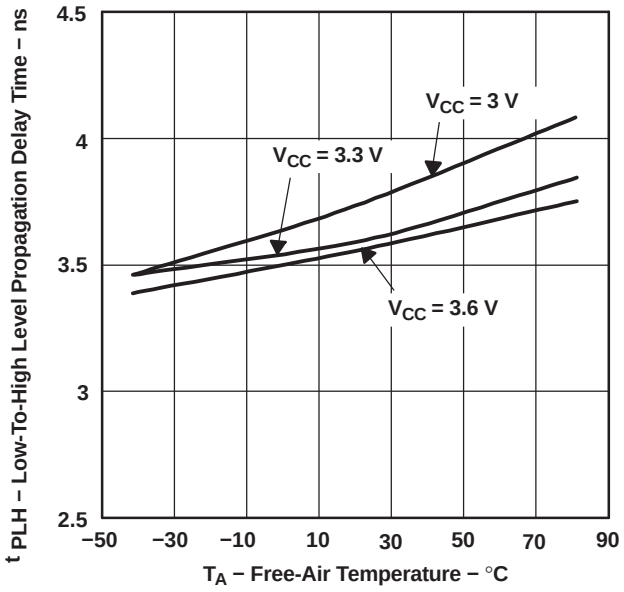


Figure 15.

APPLICATION INFORMATION

Equipment

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS7404 Real Time Scope
- Agilent ParBERT E4832A

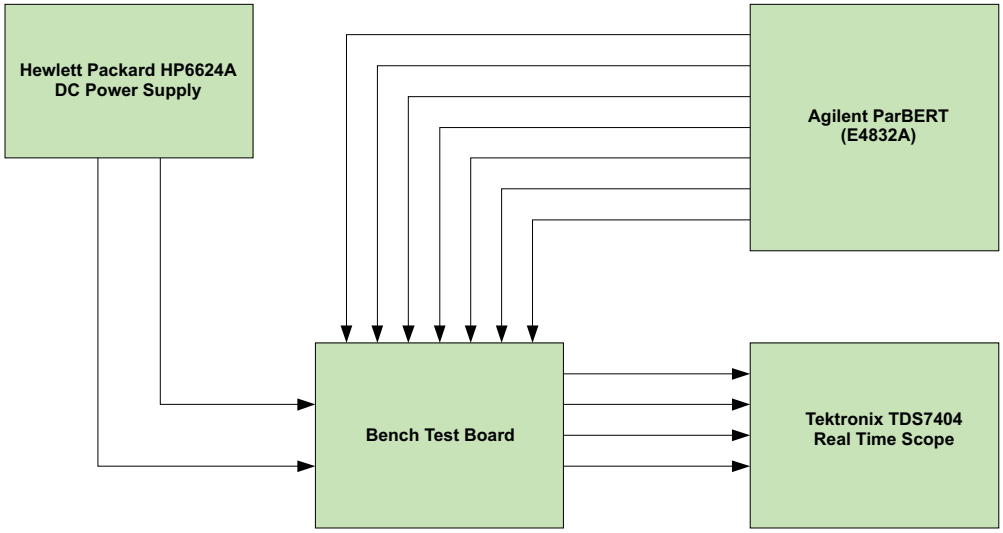
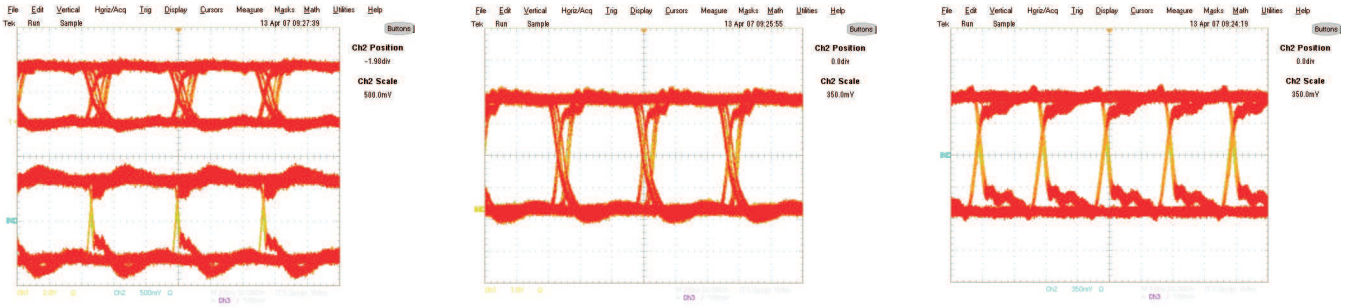


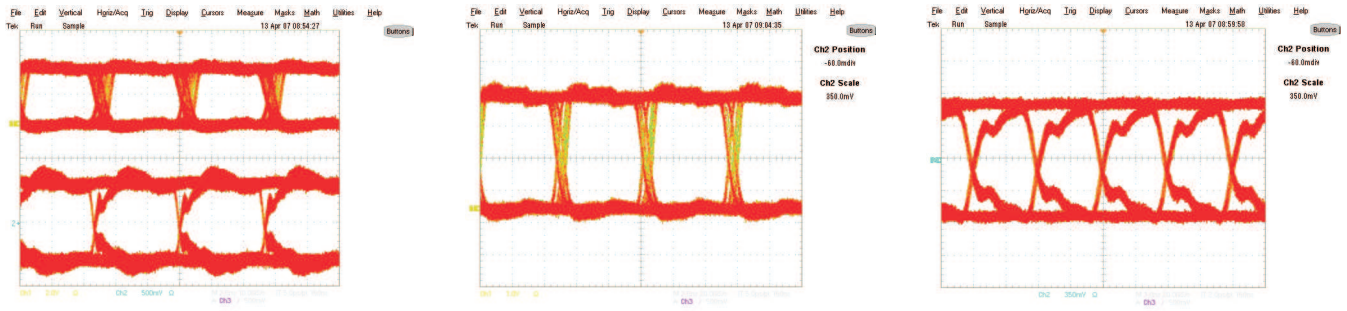
Figure 16. Equipment Setup



(a) **(b)** **(c)**

a. Tx + Rx running at 150 Mbps; Channel 1: R, Channel 2: Y-Z
b. Rx only running at 150 Mbps; Channel 1: R
c. Tx only running at 500 Mbps; Channel 1: Y-Z

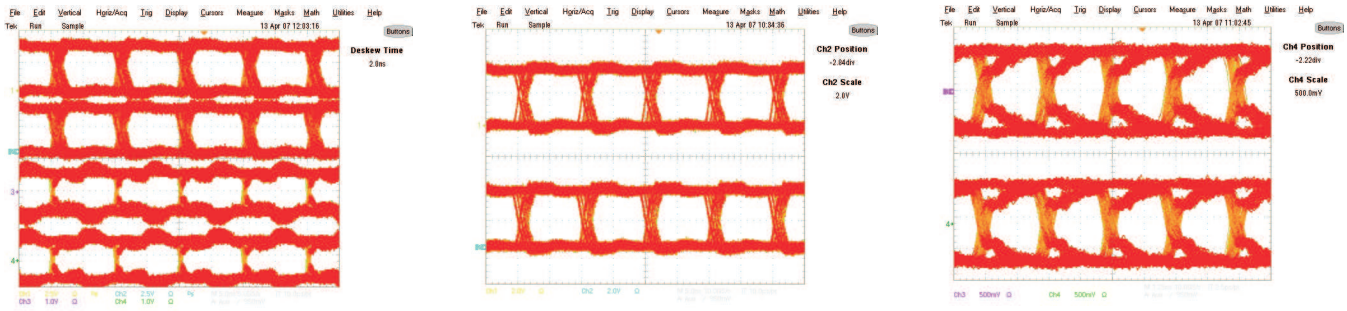
Figure 17. Typical Eye Patterns SN65LVDM179: (T = 25°C; V_{CC} = 3.6 V; PRBS = 2^{23-1})



(a) (b) (c)

a. Tx + Rx running at 150 Mbps; Channel 1: R, Channel 2: Y-Z
b. Rx only running at 150 Mbps; Channel 1: R
c. Tx only running at 500 Mbps; Channel 1: Y-Z

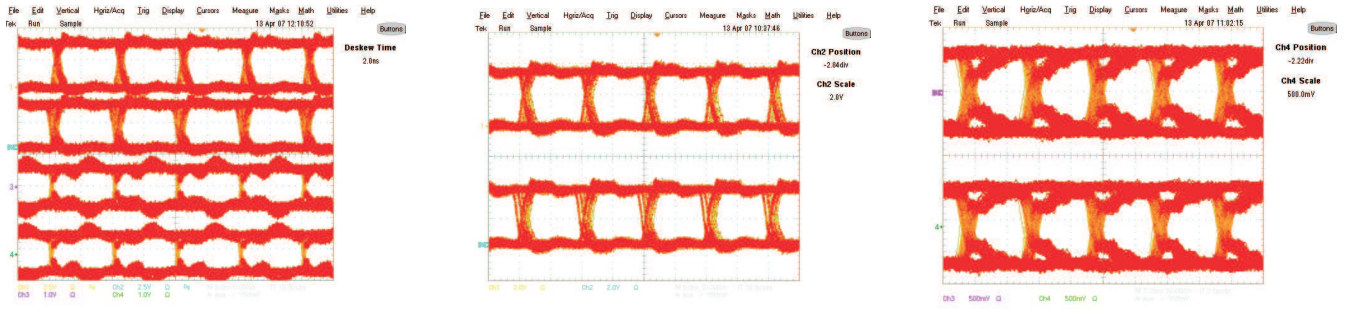
Figure 18. Typical Eye Patterns SN65LVDM180: (T = 25°C; V_{CC} = 3.6 V; PRBS = 2^{23-1})



(a) (b) (c)

a. All buffers running at 100 Mbps; Channel 1: R, Channel 2: 2R, Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,
b. Rx buffers only running at 100 Mbps; Channel 1: R, Channel 2: 2R
c. Tx buffers only running at 400 Mbps; Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,

Figure 19. Typical Eye Patterns SN65LVDM050: (T = 25°C; V_{CC} = 3.6 V; PRBS = 2^{23-1})



(a) (b) (c)

a. All buffers running at 100 Mbps; Channel 1: R, Channel 2: 2R, Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,
b. Rx buffers only running at 100 Mbps; Channel 1: R, Channel 2: 2R
c. Tx buffers only running at 400 Mbps; Channel 3: 1Y-1Z, Channel 4: 2Y-2Z,

Figure 20. Typical Eye Patterns SN65LVDM051: (T = 25°C; V_{CC} = 3.6 V; PRBS = 2^{23-1})

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers maintain ECL speeds without the power and dual supply requirements.

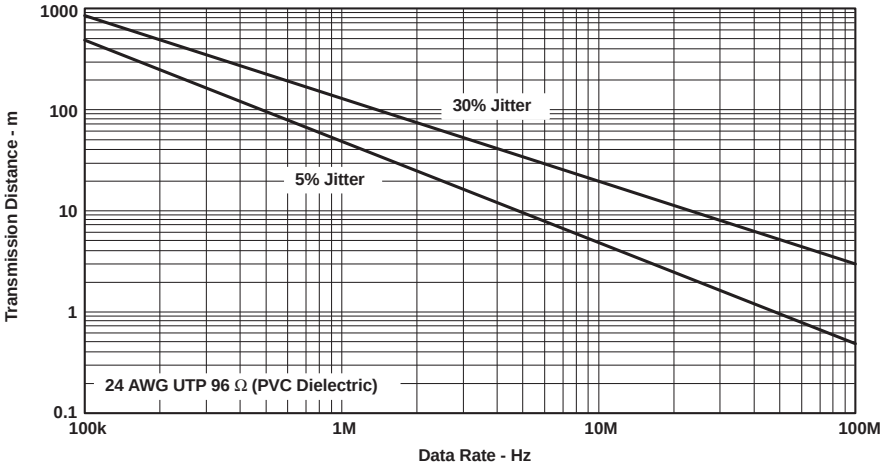


Figure 21. Data Transmission Distance Versus Rate

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different; however, in the way it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 22. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to V_{CC} – 0.4 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

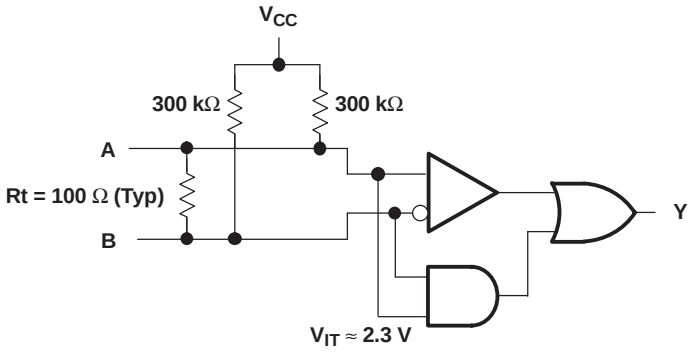


Figure 22. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, R_t, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

REVISION HISTORY

Changes from Revision I (January 2009) to Revision J	Page
• Changed value from 40 to -40	4
• Deleted value 85 from NOM value and moved to max	4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDM050D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050DG4.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM050PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM050
SN65LVDM051D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM051PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM051
SN65LVDM179D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM179
SN65LVDM179D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM179
SN65LVDM179DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM179
SN65LVDM179DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M79
SN65LVDM179DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M79
SN65LVDM179DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	M79
SN65LVDM179DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M79
SN65LVDM179DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM179
SN65LVDM179DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM179
SN65LVDM179DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM179

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDM180D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180D.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180DG4.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180PW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180PWG4.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180
SN65LVDM180PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM180

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDM050, SN65LVDM051 :

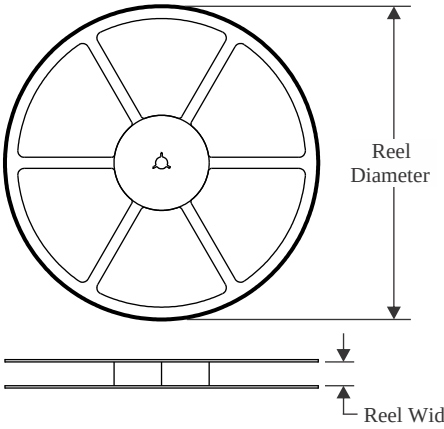
- Automotive : SN65LVDM050-Q1, SN65LVDM051-Q1

NOTE: Qualified Version Definitions:

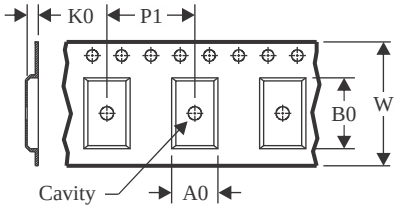
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

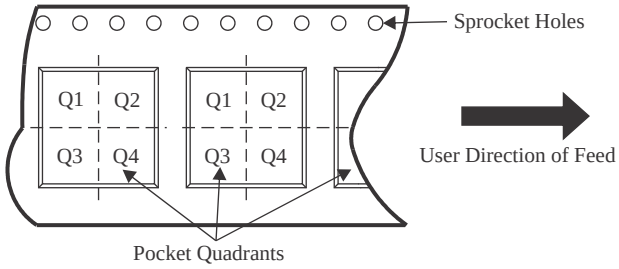


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

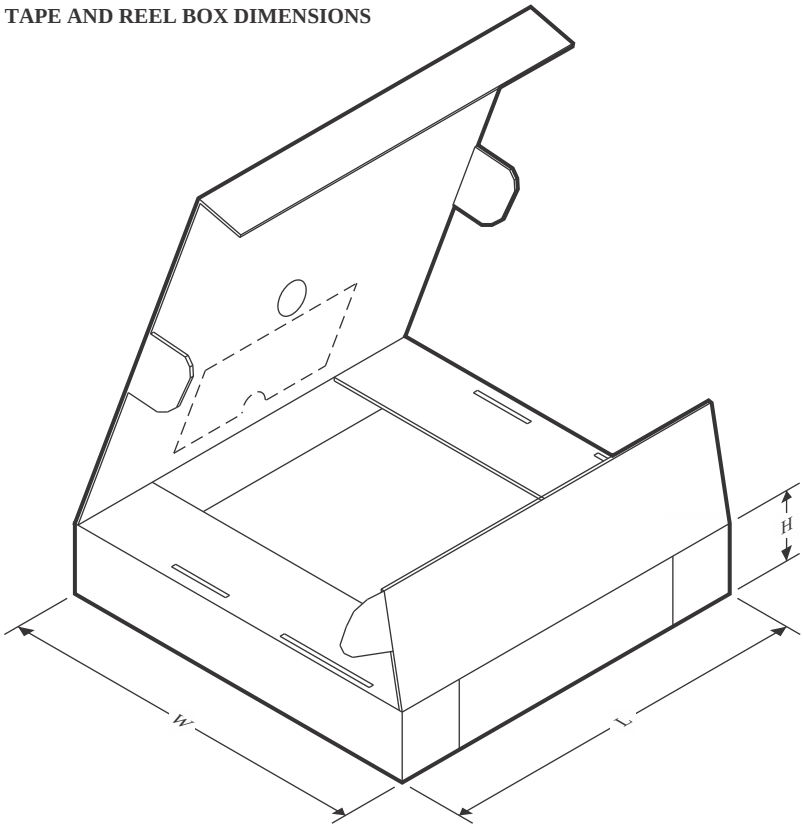
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDM050DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDM050PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDM051DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDM051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDM179DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDM179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDM179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDM180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LVDM180PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

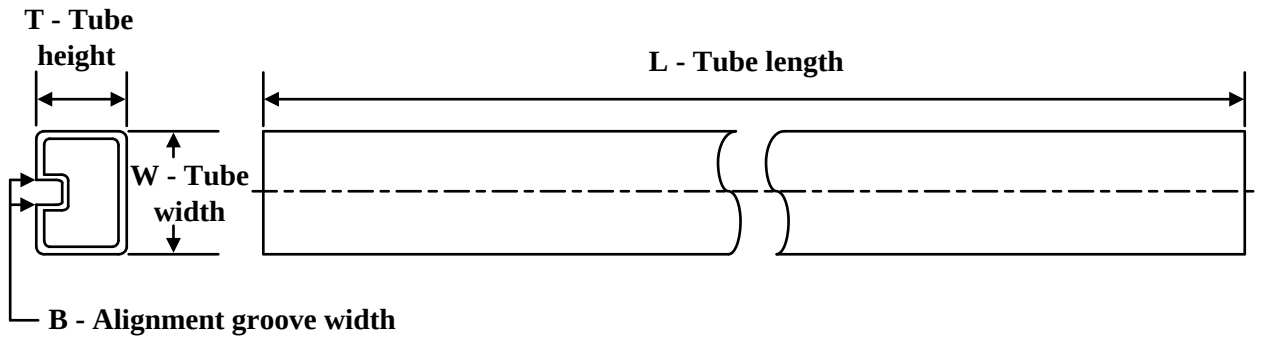
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDM050DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDM050PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDM051DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDM051PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDM179DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
SN65LVDM179DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65LVDM179DR	SOIC	D	8	2500	350.0	350.0	43.0
SN65LVDM180DR	SOIC	D	14	2500	350.0	350.0	43.0
SN65LVDM180PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

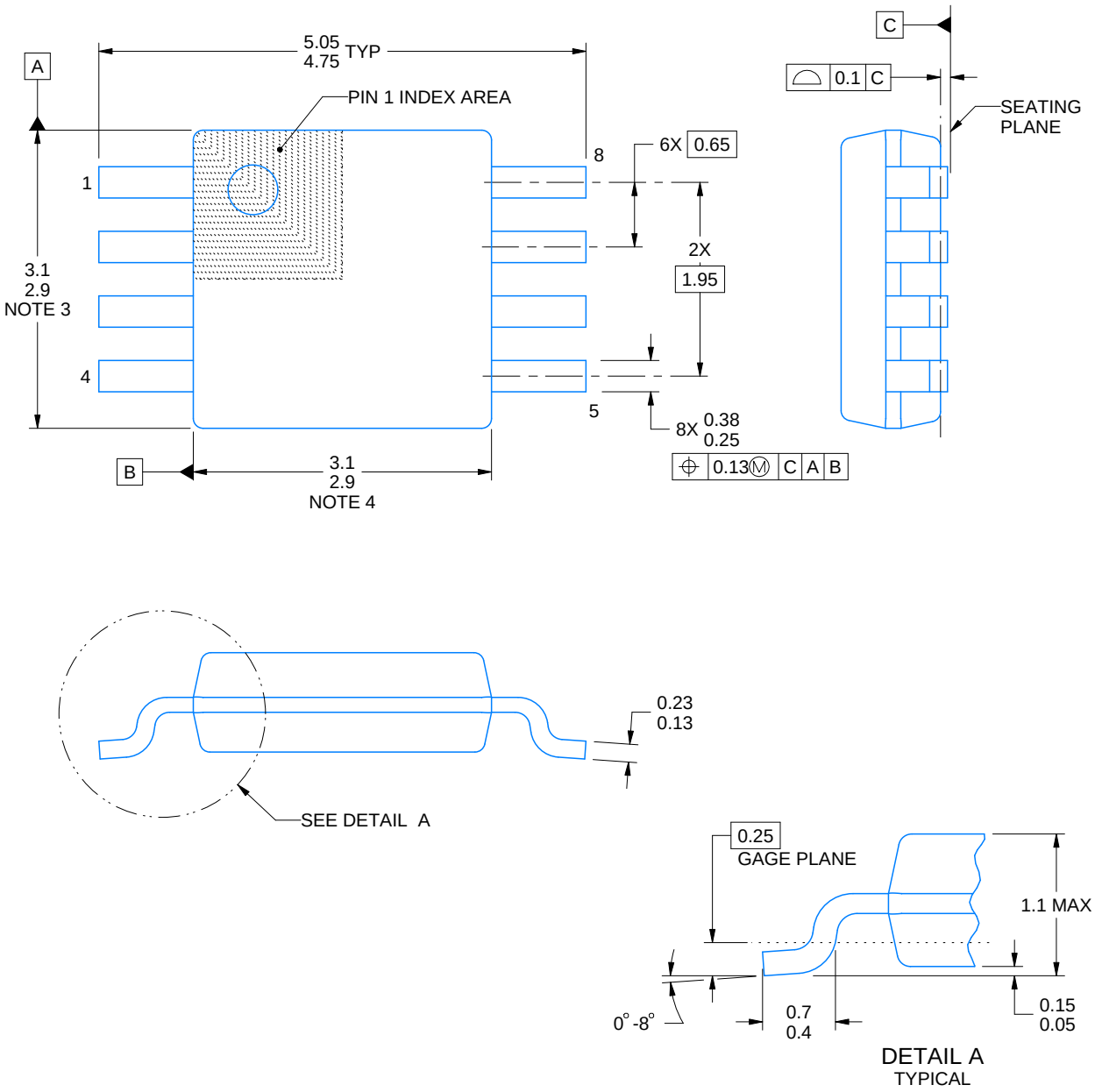
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDM050D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM050D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM050DG4.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM050PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDM050PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDM051D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM051D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM051DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM051PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDM051PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDM179D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDM179D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDM179D.B	D	SOIC	8	75	507	8	3940	4.32
SN65LVDM179D.B	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDM179DG4	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDM179DG4	D	SOIC	8	75	507	8	3940	4.32
SN65LVDM180D	D	SOIC	14	50	505.46	6.76	3810	4
SN65LVDM180D.B	D	SOIC	14	50	505.46	6.76	3810	4
SN65LVDM180DG4.B	D	SOIC	14	50	505.46	6.76	3810	4
SN65LVDM180PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN65LVDM180PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN65LVDM180PWG4.B	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

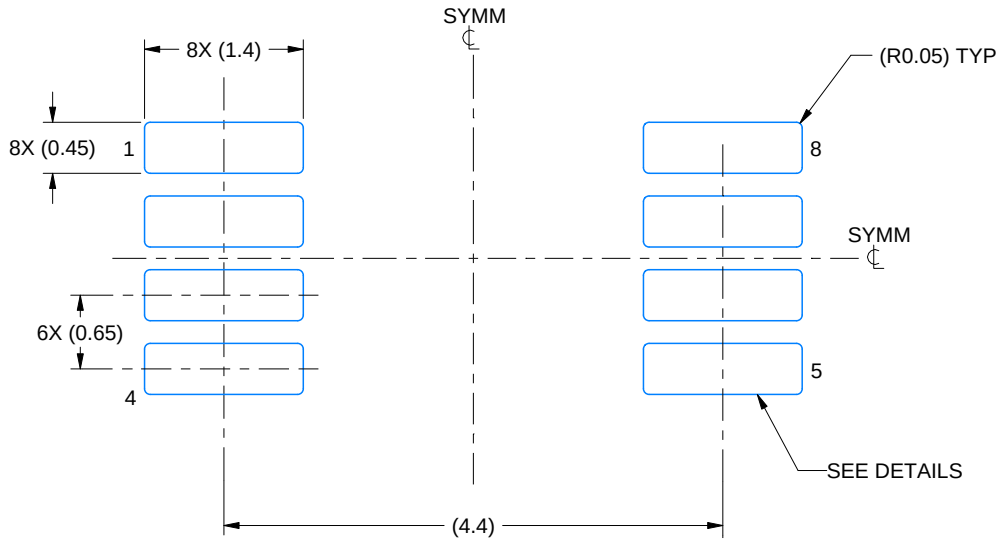
SMALL OUTLINE PACKAGE



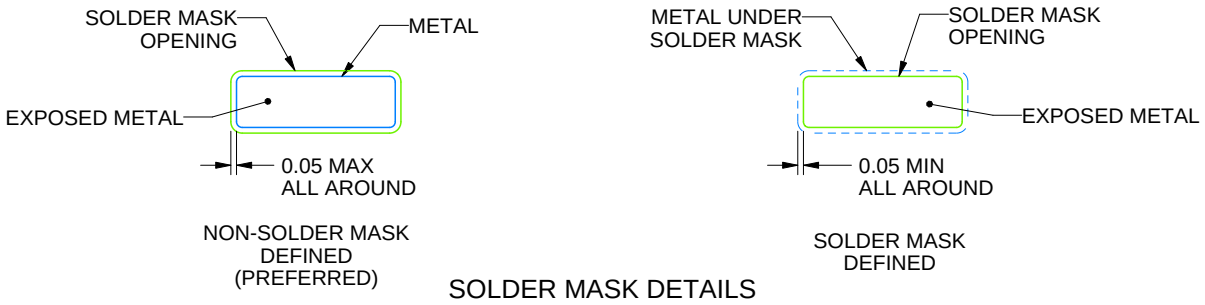
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

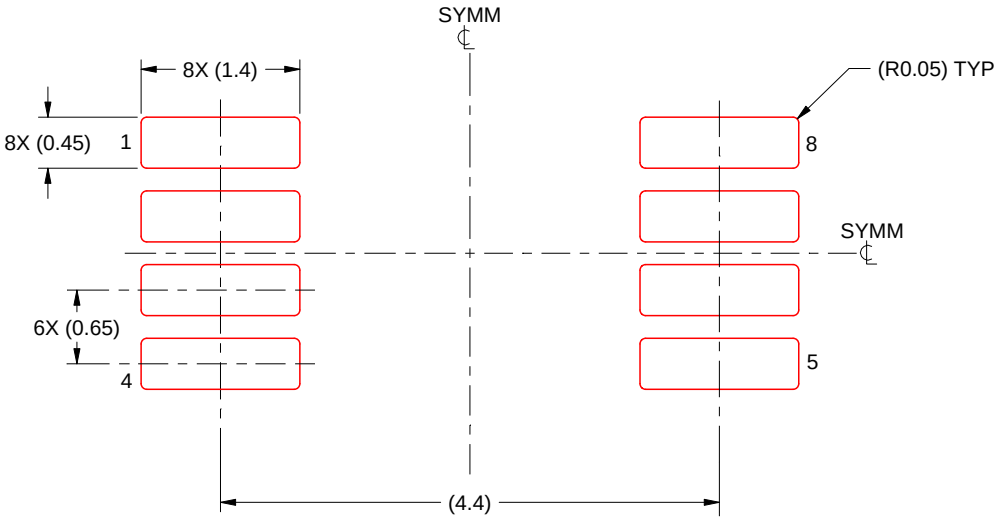


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

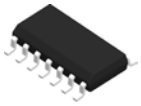


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

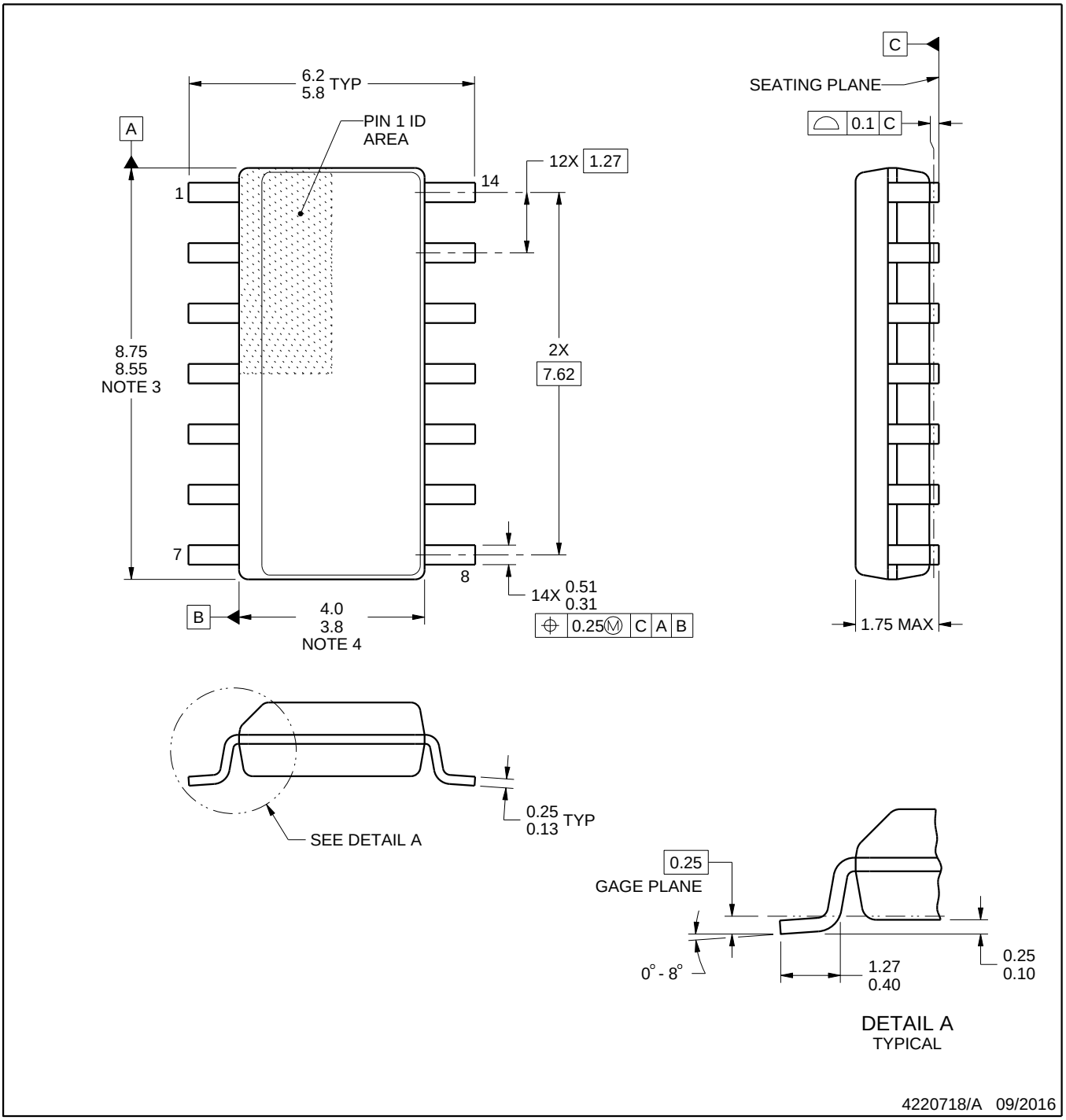


PACKAGE OUTLINE

D0014A

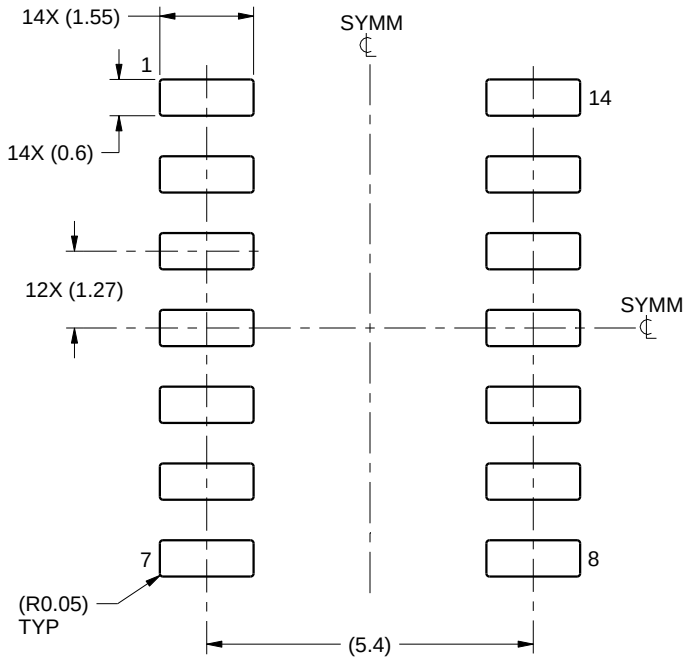
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

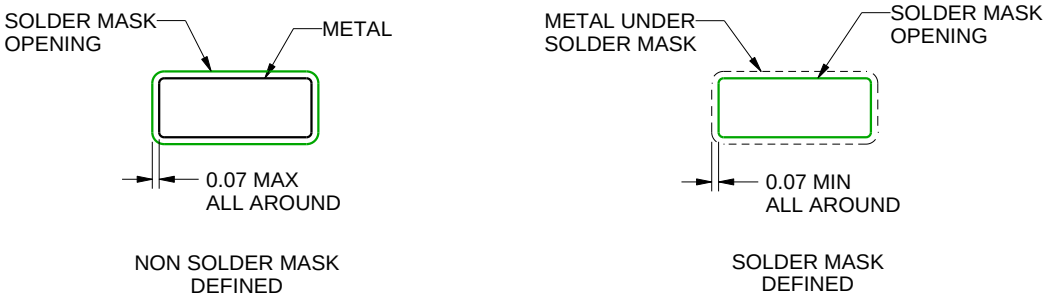


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

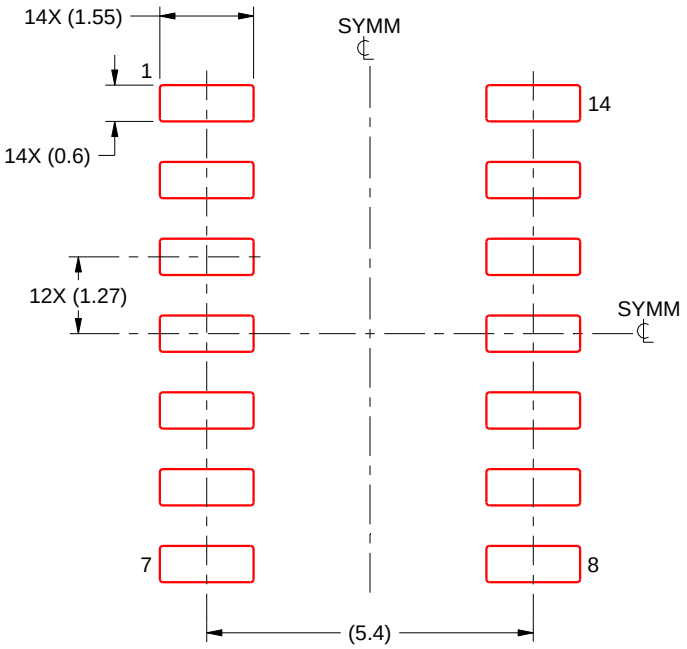
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



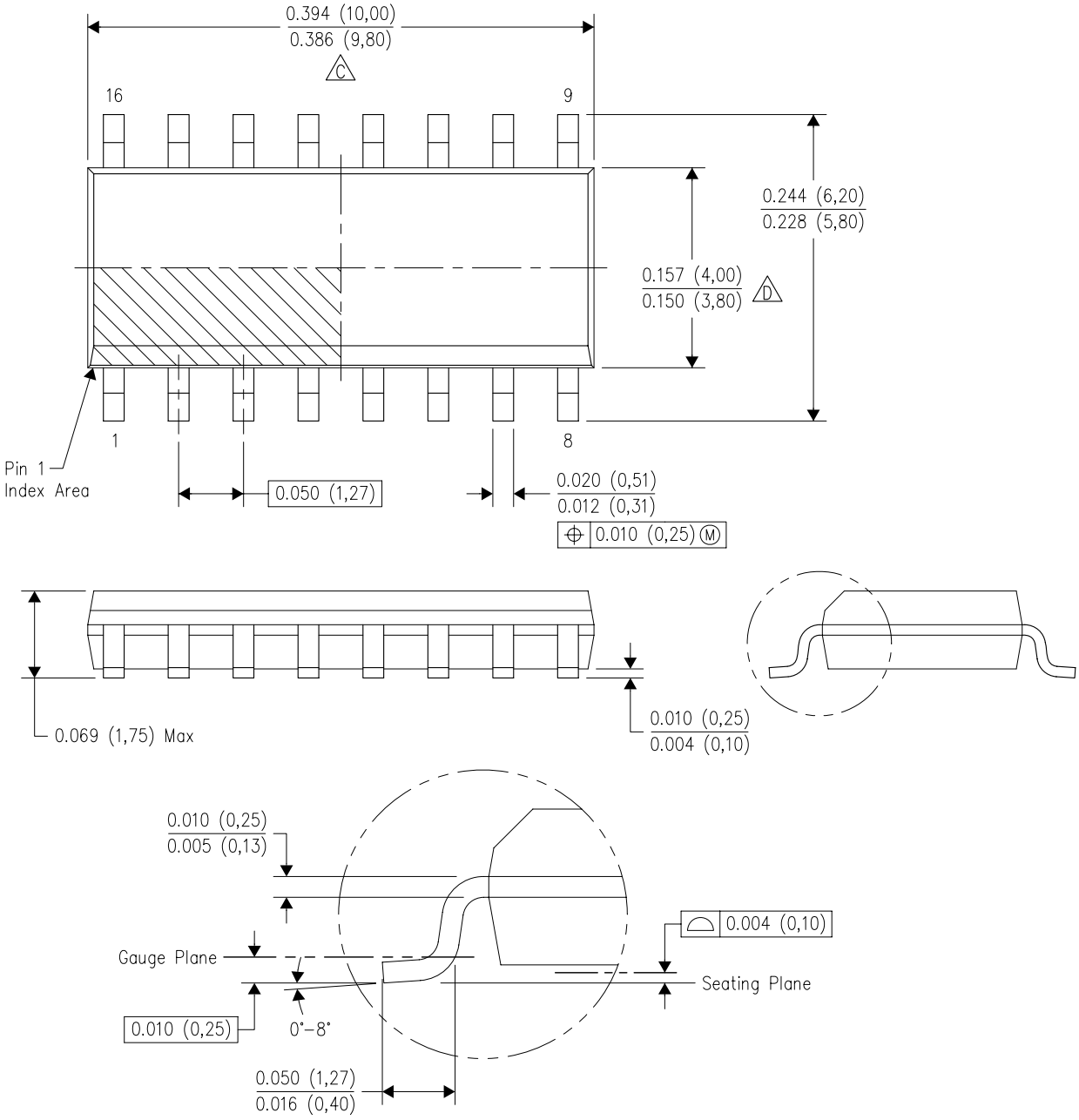
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



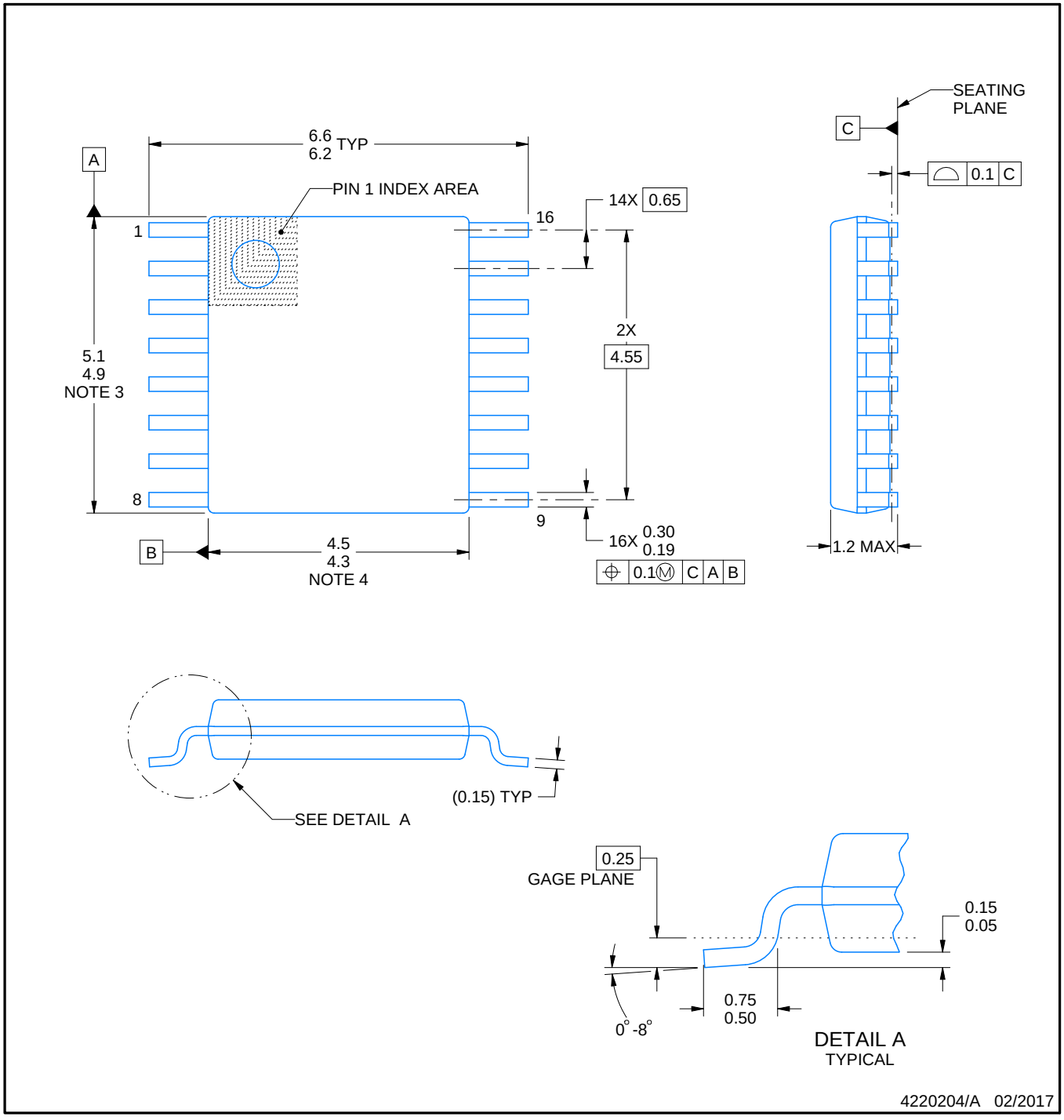
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

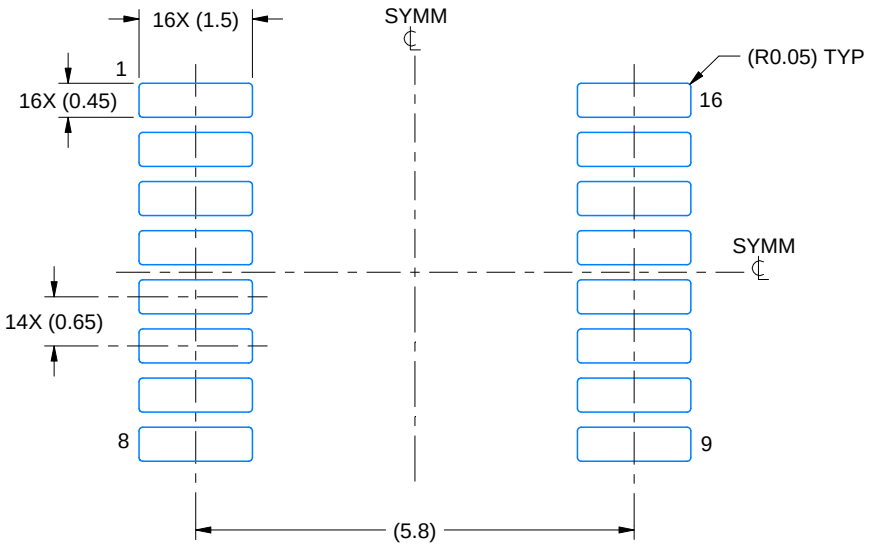
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

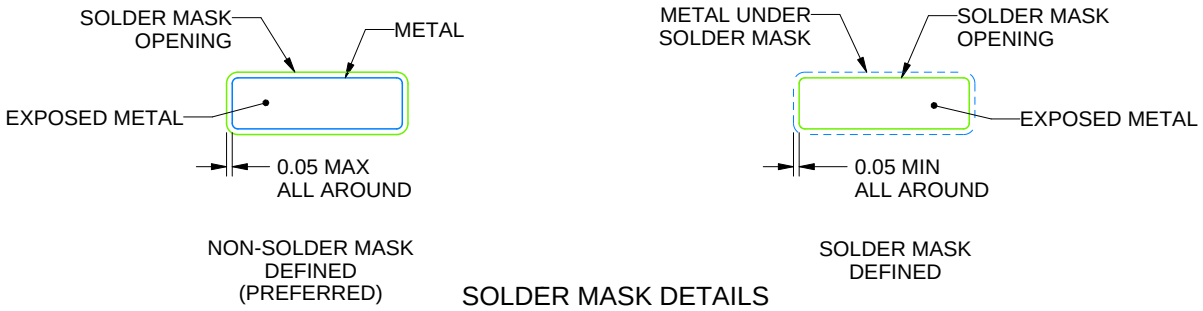


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

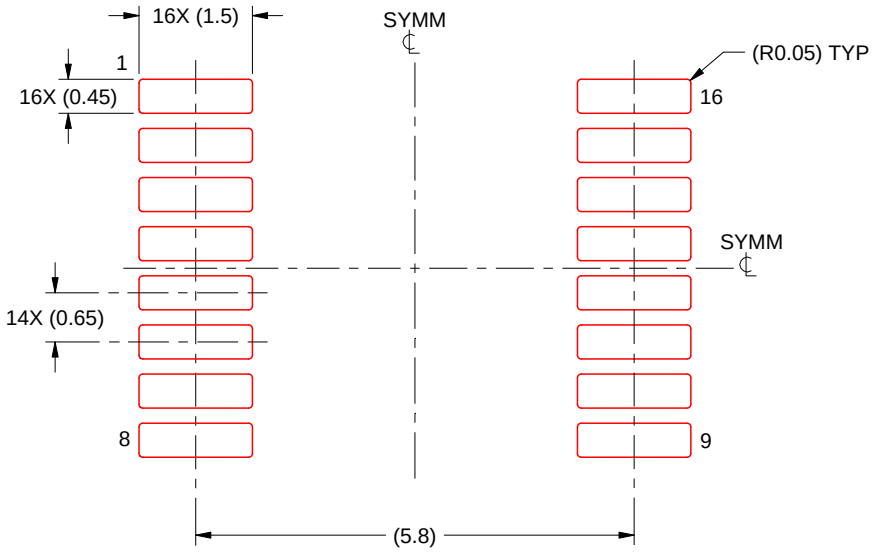


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

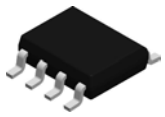


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

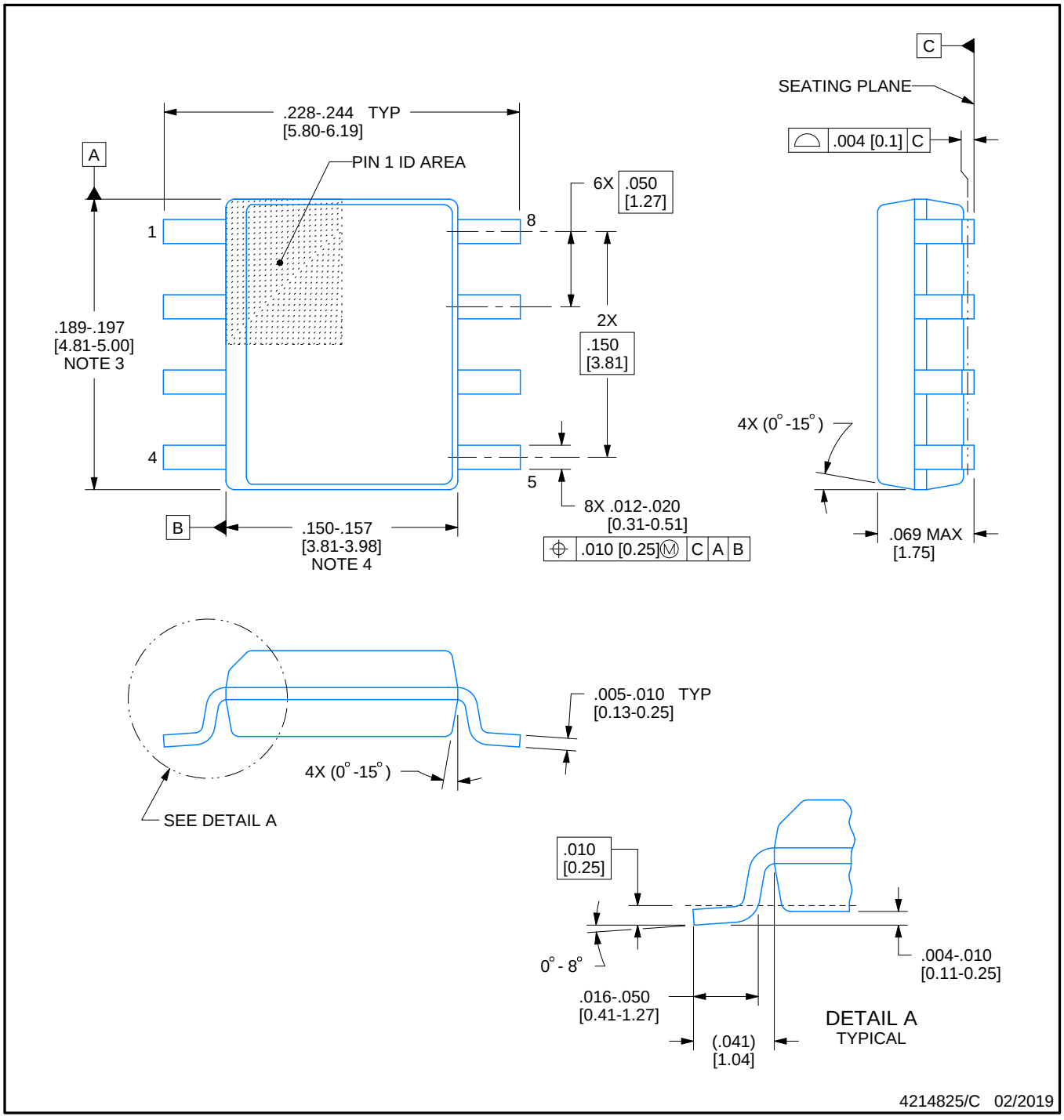


PACKAGE OUTLINE

D0008A

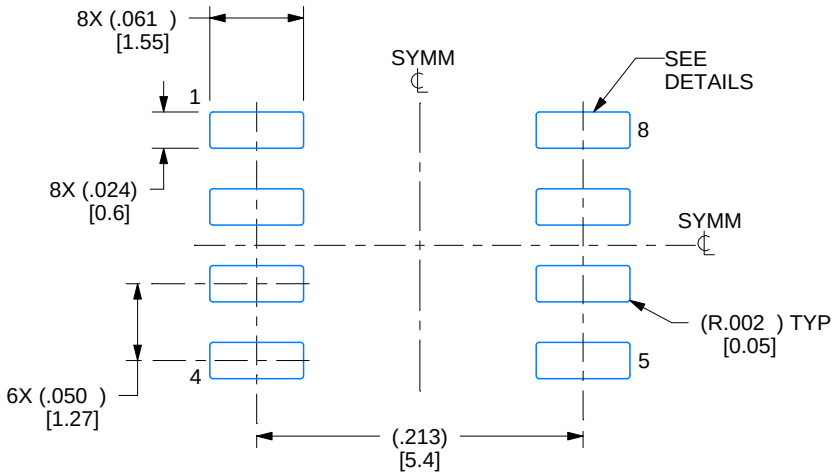
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

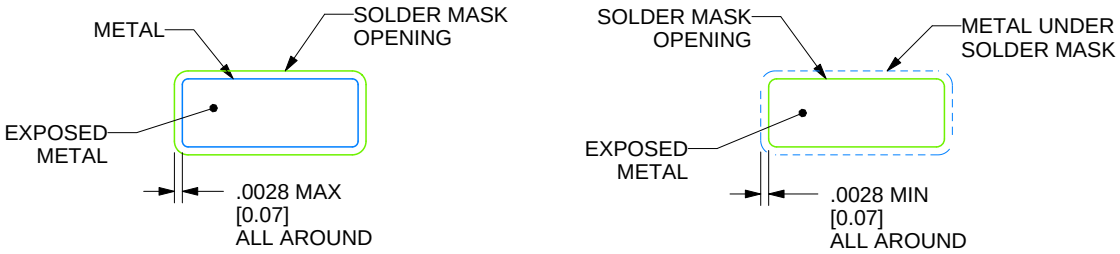


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

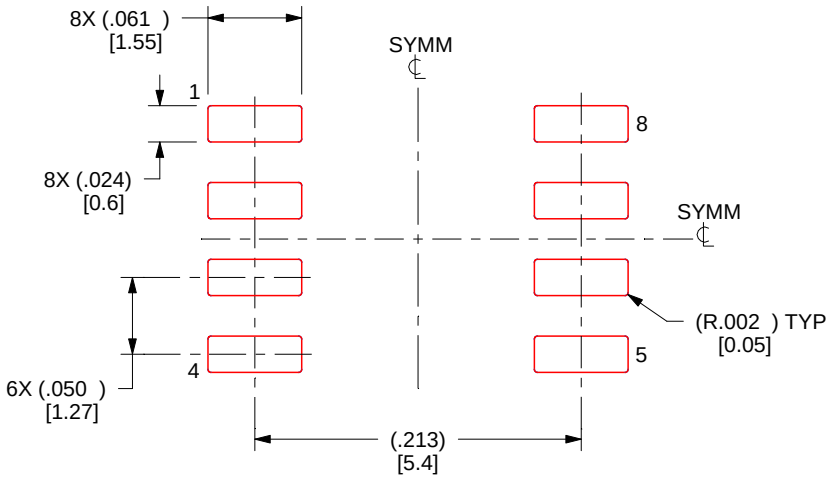
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

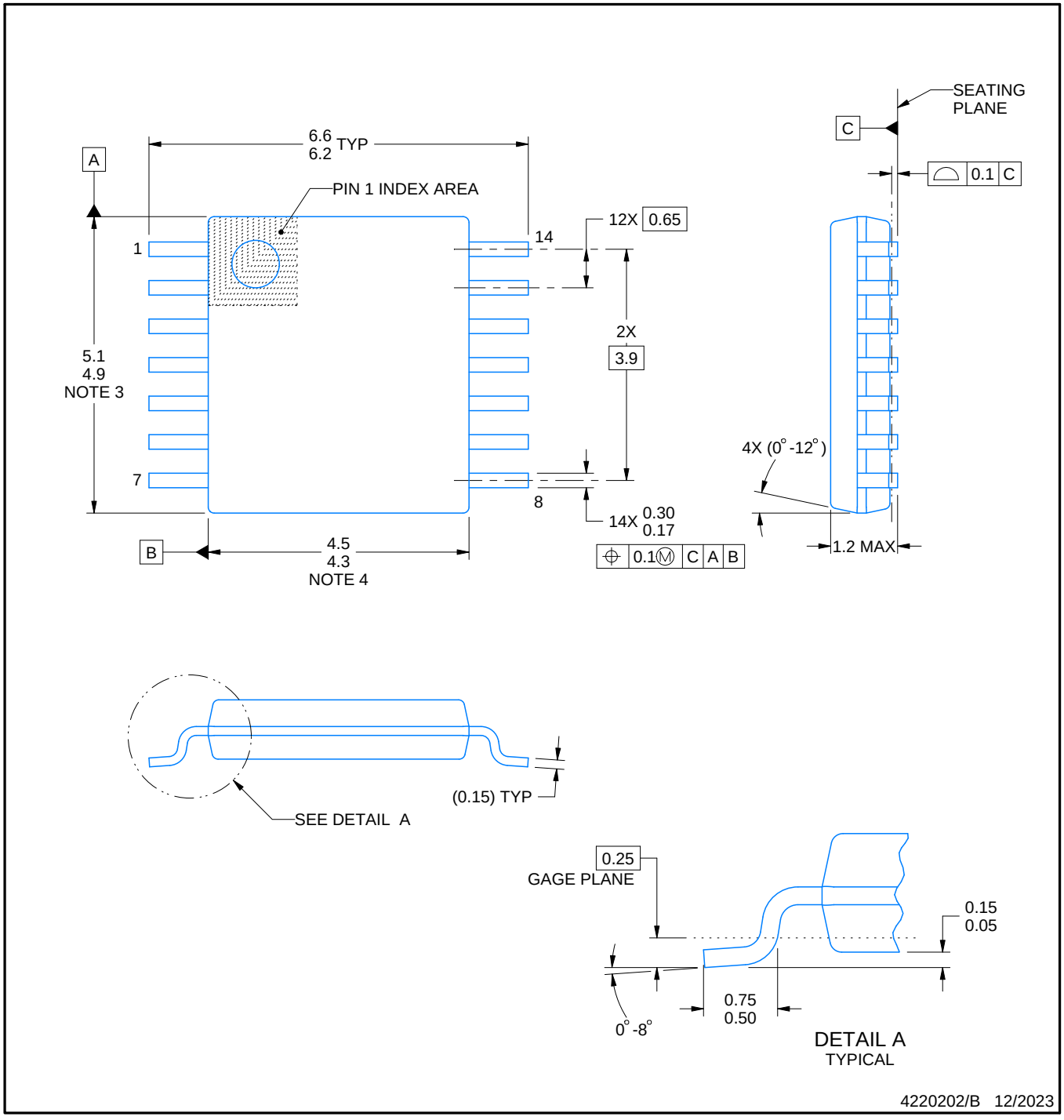
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

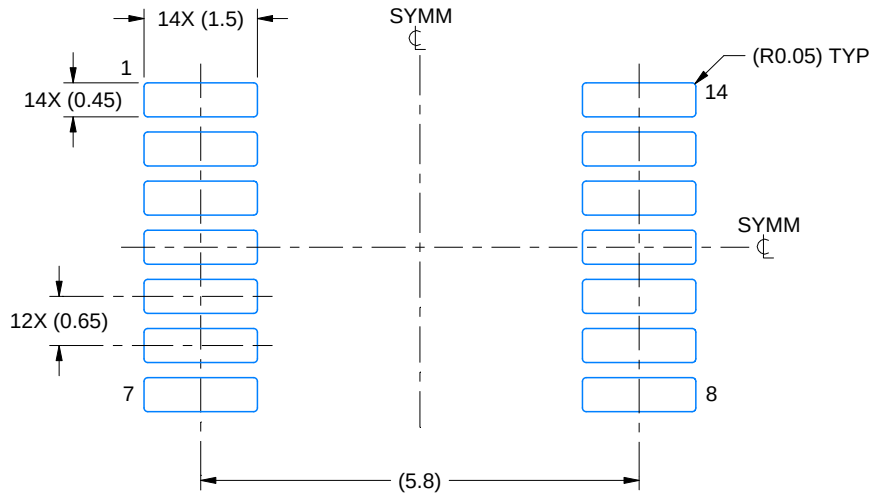
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

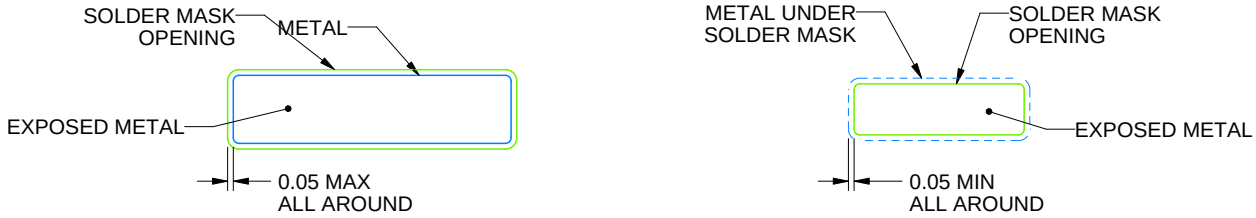


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

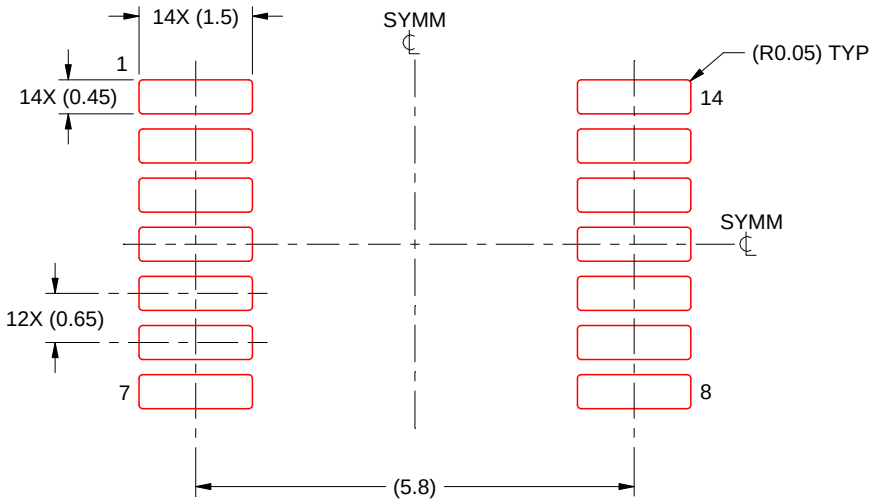


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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